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Heteroepitaxial Ge MOS Devices on Si Using Composite AlAs/GaAs Buffer

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ABSTRACT Structural and electrical characteristics of epitaxial germanium (Ge) heterogeneously integrated on silicon (Si) via a composite, large bandgap AlAs/GaAs buffer are investigated. Electrical characteristics of N-type metal-oxide-semiconductor (MOS) capacitors, fabricated from the aforementioned material stack are then presented. Simulated and experimental X-ray rocking curves show distinct Ge, AlAs, and GaAs epilayer peaks. Moreover, secondary ion mass spectrometry, energy dispersive X-ray spectroscopy (EDS) profile, and EDS line profile suggest limited interdiffusion of the underlying buffer into the Ge layer, which is further indicative of the successful growth of device-quality epitaxial Ge layer. The Ge MOS capacitor devices demonstrated low frequency dispersion of 1.80% per decade, low frequency-dependent flat-band voltage, V_{FB}, shift of 153 mV, efficient Fermi level movement, and limited C-V stretch out. Low interface state density (D_{it}) from 8.55×10^{11} to 1.09×10^{12} cm^{-2} eV^{-1} is indicative of a high-quality oxide/Ge heterointerface, an effective electrical passivation of the Ge surface, and a Ge epitaxy with minimal defects. These superior electrical and material characteristics suggest the feasibility of utilizing large bandgap III-V buffers in the heterointegration of high-mobility channel materials on Si for future high-speed complementary metal-oxide semiconductor logic applications.

INDEX TERMS Germanium (Ge), heteroepitaxy, metal-oxide semiconductor (MOS) devices, silicon (Si), III-V materials.

I. INTRODUCTION

Aggressive scaling of silicon (Si) complementary metal-oxide-semiconductor (CMOS) transistors has resulted in an exponential increase in device density, and thus computing power, over the past four decades. To mitigate the increased power consumption as a result of increasing transistor density, supply voltage scaling is essential to maintain low-power device operation, but at the cost of significantly degrading transistor drive current due to the low carrier mobility of Si [1]. Overcoming the limitations of device and voltage scaling without degrading transistor drive current requires the adoption of narrow bandgap channel materials with superior transport properties. However, the use of such materials as bulk substrates is cost-prohibitive. Thus, another key technical challenge is the heterogeneous integration of high-mobility alternative channel materials on affordable and established Si technology platform.

Germanium (Ge) is an attractive candidate for next-generation low-power devices operating at low-voltage (≤ 0.5 V) due to its high electron and high hole mobility ($2\times$ and $4\times$, respectively, as compared to those of Si) [2]. Although Ge has been successfully integrated on GaAs substrate [3]–[8], it remains an important issue to integrate Ge on to Si substrate. Thus, numerous methods for the epitaxial growth of Ge on Si have been reported in order to demonstrate the device-quality Ge as a future channel

material [9]. However, none of these methods have addressed the utilization of high conduction and valance band offsets in order to confine carriers within the Ge nor the elimination of parallel conduction within the buffer layers. Recently, we have demonstrated an innovative method to heterogeneously integrate device-quality epitaxial Ge on Si using a composite, large bandgap AlAs/GaAs buffer, where (i) the high-resistivity, large bandgap (2.15 eV) AlAs layer prevents parallel conduction to the active Ge layer, (ii) high conduction and valance band offsets between the Ge/AlAs heterojunction of ∼1 eV and ∼0.5 eV help confine electrons and holes, respectively, to the active Ge layer, and (iii) the GaAs buffer helps reduce dislocations within the active Ge layer, thereby acting as a virtual substrate for active layer integration on to the Si platform [10]. Although successful germanium on insulator (GeOI) pMOSFETs have been demonstrated [11], where the large bandgap of SiO_2 (9.1 eV) is an attractive feature for low-power applications, the GeOI approach has several shortcomings compared with the direct heterogeneous approach in this study, namely (i) GeOI via bonding of Ge wafer onto Si wafer is not economically feasible for large diameter wafer production due to the size of Ge; (ii) due to the poor thermal conductivity of SiO_2, a large density of thermal mismatch induced defects might occur inside the Ge layer due to the large difference in the thermal expansion coefficients of Ge (6×10^{-6}/K) and Si (2.6×10^{-6}/K); and (iii) GeOI wafers formed using the thermal-cut method results in non-uniform variation of Ge layer thicknesses. Thus, the AlAs/GaAs epilayers can act as a common buffer platform for next-generation n- and p-Ge CMOS devices heterogeneously integrated on Si. *In this paper*, we report on the structural characteristics of the Ge epitaxial layer heterogeneously integrated on Si using a composite III-V AlAs/GaAs buffer and on the electrical characteristics of metal-oxide-semiconductor capacitors (MOS-Cs) fabricated from the aforementioned material stack.

II. EXPERIMENT

The 240 nm of unintentionally doped (UID) epitaxial Ge was grown *in-situ* on a composite III-V buffer heterogeneously integrated on (100) Si substrate with 6° offcut by solid source molecular beam epitaxy utilizing separate Ge and III-V growth chambers connected *via* an ultra-high vacuum transfer chamber. The lattice-matched, composite III-V buffer consist of (i) a large bandgap 170 nm AlAs barrier layer and (ii) a 2.2 μm GaAs virtual substrate. Epitaxial Ge was grown at 400°C at a growth rate of ∼ 0.1Å/s in order to minimize interdiffusion between the epitaxial Ge and the underlying AlAs/GaAs buffer layers. The Ge sheet concentration, as determined by Hall measurements utilizing the Van der Pauw technique, was measured to be on the order of 10^{14} cm^{-2}. Further details of the material growth are reported elsewhere [10].

N-type MOS-Cs were fabricated on the epitaxial Ge material stack. Fabrication of the devices began with a degrease

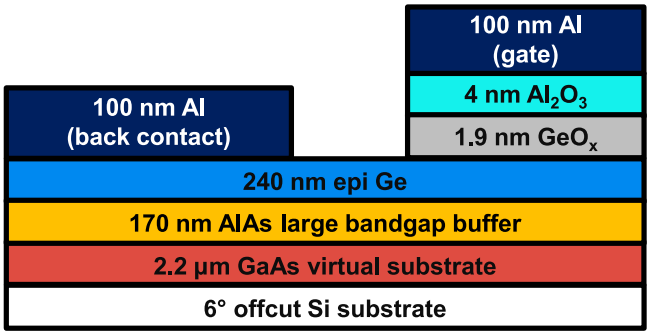

FIGURE 1. Cross-sectional schematic of the Al/Al_2O_3/GeOx/Ge MOS-C on Si via a composite AlAs/GaAs buffer architecture.

using acetone, isopropanol, and deionized (DI) water, followed by a three minute native oxide removal in dilute (1:10) hydrofluoric acid. A high-quality, native GeO_x interfacial passivating layer was then formed by thermal oxidation at 450°C for 10 minutes in an O_2 ambient. Immediately afterwards, a 4 nm Al_2O_3 gate oxide was deposited at 250°C using a Cambridge NanoTech atomic layer deposition (ALD) system with trimethylaluminum and DI water as precursors for Al and oxygen, respectively. The 100 nm Al gate electrodes and ohmic contacts were subsequently deposited using a Kurt J. Lesker PVD250 electron beam deposition chamber. The devices were then annealed at 250°C in forming gas (N_2:H_2 95%:5%) for two minutes. Fig. 1 shows a cross-sectional schematic of the Ge MOS-C device structure.

The structural quality and relaxation state of the epitaxial Ge and underlying AlAs/GaAs buffer were evaluated by high-resolution triple-axis x-ray rocking curve from high-resolution x-ray diffraction (HR-XRD) using a Panalytical X-pert Pro system equipped with both PIXel and proportional detectors. Panalytical Epitaxy simulation software was used to simulate the triple-axis x-ray rocking curve. Dynamic secondary ion mass spectrometry (SIMS) was used to determine the depth profile of Al, As, Ga, Ge, and Si atoms at the interfaces of the Ge/AlAs/GaAs heterostructure grown on Si substrate. The SIMS analysis was performed using a Cameca IMS-7f GEO with 5 kV Cs^+ bombardment and MCs^+ detection to reduce matrix effects. To analyze the elemental composition of the Ge/AlAs/GaAs heterostructure grown on Si substrate, energy dispersive x-ray spectroscopy (EDS) was performed using a JEOL 2100 transmission electron microscope (TEM) operating in scanning TEM mode. The electron transparent foils required for EDS were prepared by mechanical polishing and subsequent low-temperature Ar^+ ion beam milling.

Low- and room-temperature multi-frequency capacitance-voltage (C-V) and conductance-voltage (G-V) measurements of the Ge MOS-Cs were performed using an HP4284A precision LCR meter with frequencies ranging from 1 kHz to 1 MHz. Accurate measurements were obtained with the removal of series resistance, as discussed in [12].

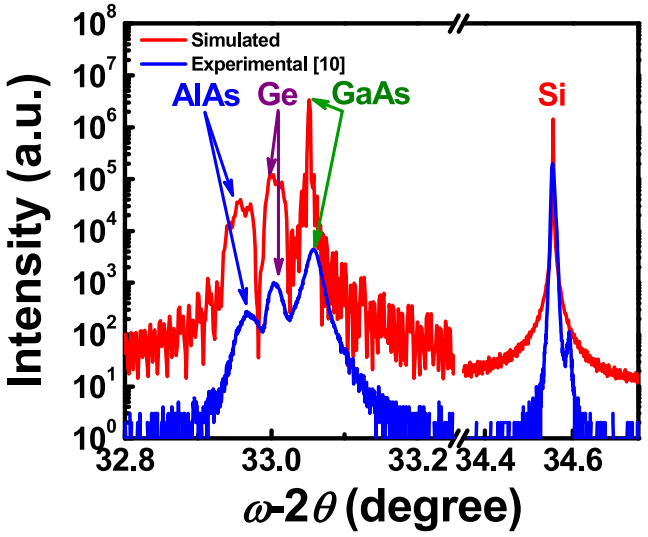

FIGURE 2. Simulated (red) and experimental [10] (blue) symmetric (004) X-ray rocking curve of the Ge/AlAs/GaAs heterostructure grown on Si substrate.

TCAD Sentaurus software was used to simulate high-frequency C-V curves to compare against the experimental data. To study the structural quality of the MOS-C interfaces, cross-sectional high-resolution TEM was performed using a JEOL 2100 TEM. The foils prepared for EDS were also used for cross-sectional high-resolution TEM.

III. RESULTS AND DISCUSSION

A. STRAIN RELAXATION PROPERTIES

To determine the structural quality and relaxation state of the epitaxial Ge active layer on AlAs/GaAs buffer layers grown on Si, high-resolution triple-axis x-ray (004) rocking curves were measured. Fig. 2 shows both experimental and simulated symmetric (004) rocking curve for the Ge/AlAs/GaAs heterostructure grown on Si [10]. From the experimental rocking curve, shown in blue in Fig. 2, distinct peaks of the Ge, AlAs, and GaAs layers, with angular separations resulting from differences in their respective lattice plane spacing, are clearly observed. The GaAs is almost fully relaxed with respect to Si and thus, serves as a virtual substrate for the epitaxial Ge. Additionally, the quasi-lattice-matched nature of the Ge, AlAs, and GaAs layers is confirmed due to the Ge and AlAs peak positions with respect to GaAs. A simulated rocking curve, shown in red in Fig. 2, shows distinct Ge, AlAs, and GaAs peaks fitting well with the experimental peaks. The small peak on the right side of the experimentally measured Si peak is due to a measurement artifact. To ensure accuracy of the peak positions, the simulation takes into account the quasi-lattice matched nature ($\sim$0.07% lattice mismatch) of the Ge/GaAs heterostructure. However, the simulation also assumes that the AlAs/GaAs buffer layer is *fully* relaxed with respect to Si. Thus, the simulated GaAs peak has a much narrower full width at half maximum as compared to that in the experimental measurement. Furthermore, the close proximity of the measured and simulated full width at half maximums (69.7 arcsec and 79.5 arcsec, respectively), where the simulation assumes a perfect Ge epitaxy, demonstrates that high-quality epitaxial Ge film growth was achieved.

B. SIMS DEPTH PROFILE AND EDS ANALYSIS

Dynamic SIMS depth profiling provides insight into the extent of elemental diffusion between the epitaxial Ge active layer and the underlying AlAs/GaAs buffer layers grown on Si. Higher growth temperature promotes diffusion of adatoms across surfaces and heterointerfaces. Thus, a low Ge growth temperature (400°C) was selected to allow epitaxial Ge growth with negligible interdiffusion of species at the Ge/AlAs heterointerface [10]. Low Ge growth temperatures ($\leq$ 450°C) have been demonstrated to yield high-quality Ge epitaxial films with limited interdiffusion between the Ge and corresponding buffer layers [5]. Such optimization of Ge growth temperatures minimizes the alteration of the doping characteristics of the undoped Ge layer as a result of interdiffusion of species in the underlying buffer layers. Fig. 3(a) shows the Ge, Al, As, Ga, and Si compositional profiles in the Ge/AlAs/GaAs heterostructure grown on Si substrate. Constant Ge, Al, As, and Ga intensities within each layer demonstrates good growth uniformity of the epitaxial Ge layer as well as the underlying AlAs and GaAs buffer layers. Moreover, very low levels of Al, As, and Ga are detected within the Ge and a sharp, abrupt Ge/AlAs heterointerface is observed. The apparent interdiffusion between each interface is due to cascade mixing and the matrix effect during SIMS analysis. Thus, both Ge outdiffusion into the underlying AlAs buffer layer as well as indiffusion of Al, As, and Ga into the Ge layer are minimal, further reinforcing the successful growth of a high-quality Ge epitaxial layer on AlAs/GaAs buffer layers grown on Si.

To obtain further insight into the elemental distribution and growth behavior of the Ge/AlAs/GaAs heterostructure grown on Si, EDS elemental mapping was performed. Fig. 3(b) shows a three-element overlay of Ge, Al, and Ga, where the red corresponds to the Ge content, blue corresponds to the Al content, and green corresponds to the Ga content. Four distinct, uniform color regions corresponding to the Ge (red), AlAs (blue), GaAs (green), and Si (black) layers are clearly visible with no evidence of interdiffusion between the heterointerfaces, which would have been signified by a mixing of colors. Fig. 3(c) shows the EDS line profile of the same Ge/AlAs/GaAs heterostructure, which depicts sharp transitions between the heterostructures as well as low levels of Al, As, and Ga within the epitaxial Ge layer. The apparent rise in the Ge and Si signal is an artifact of the EDS line profile scan.

C. MOS CAPACITOR TEM

The structural quality of the oxide and Ge surface was investigated by HR-TEM. The TEM micrograph shown in Fig. 4 shows an atomically abrupt and uniform oxide-Ge heterointerface, suggesting minimal interdiffusion across

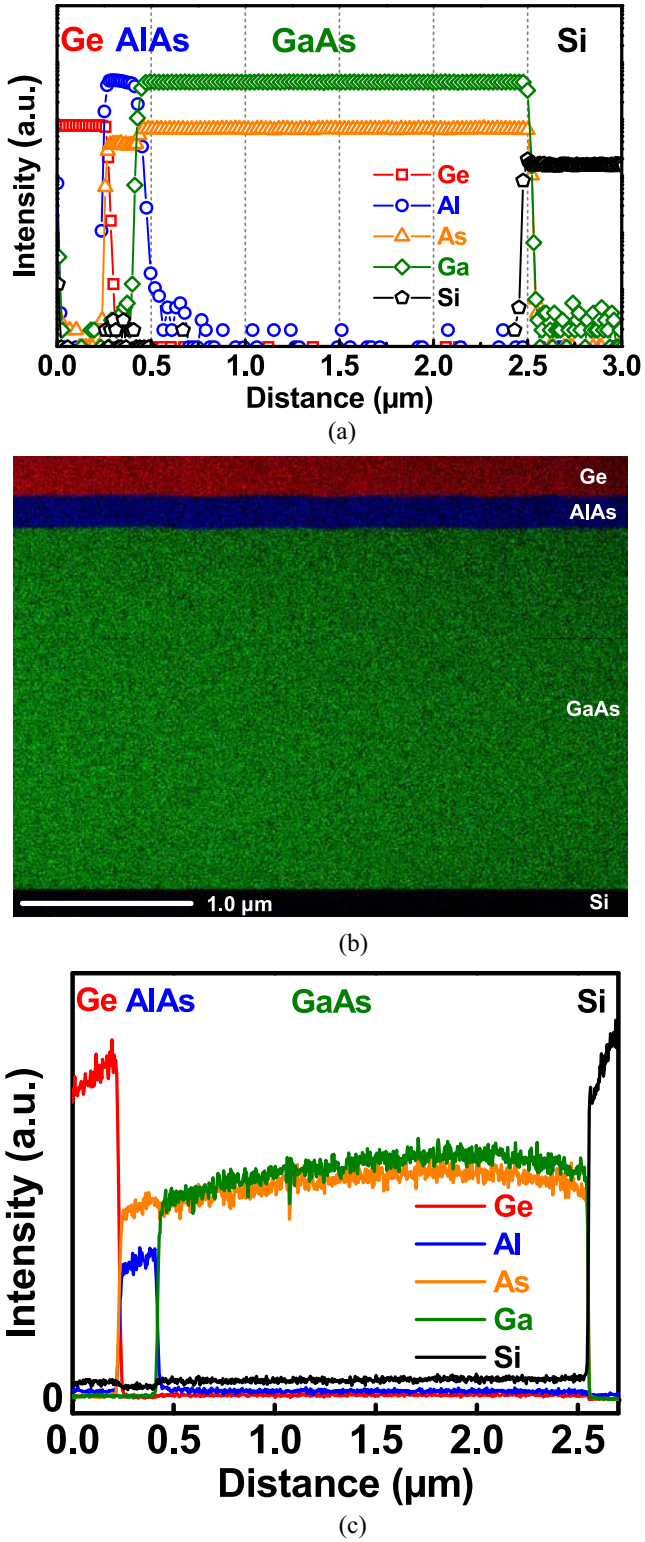

FIGURE 3. (a) SIMS profile. EDS (b) elemental mapping and (c) line profile of the Ge/AlAs/GaAs heterostructure grown on Si.

the interface, thereby minimizing the creation of interfacial defect states that would deleteriously affect device performance. Due to the low contrast in the TEM micrograph, there is no clear distinction between the ALD deposited Al_2O_3 and

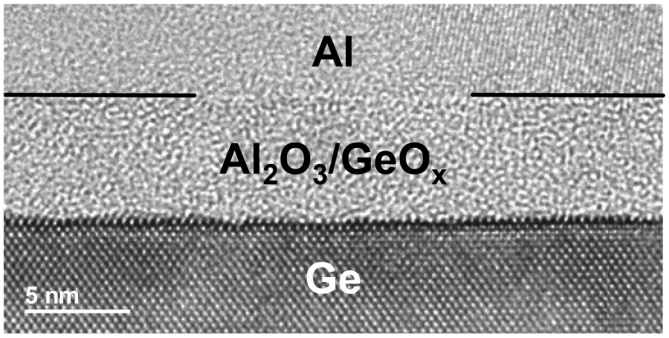

FIGURE 4. Cross-sectional TEM micrograph of the oxide-Ge heterointerface of the $Al/Al_2O_3/GeO_x/Ge$ MOS-C on Si via a composite AlAs/GaAs buffer architecture after post-metal annealing.

the thermally grown GeO_x layer shown in Fig. 4. The total thickness of the bilayer oxide is about 5.9 nm, yielding an approximate GeO_x thickness of 1.9 nm.

D. MOS CAPACITOR C-V AND CONDUCTANCE CHARACTERISTICS

Fig. 5(a)–(c) shows the C-V characteristics of the Ge MOS-C at (a) 89 K, (b) 150 K, and (c) 300 K, respectively. The low-frequency weak inversion response due to minority carriers, a feature of narrow bandgap materials, is suppressed at 89 K, thus resembling room temperature Si MOS C-V characteristics [13]. A moderate flat-band voltage (V_{FB}) shift in the overall C-V curves was observed across all temperatures, which was attributed to the high UID of the epitaxial Ge, as previously reported [10]. The devices demonstrated hysteresis in the 100 kHz C-V measurements of 0.485 V at 300 K, which reduces to 0.165 V at 89 K. The large hysteresis is a result of bulk oxide traps and is not related to the passivation of the oxide/Ge heterointerface [14], [15]. Furthermore, the bulk oxide traps may be due to different deposition techniques of high-k oxides, where the hysteresis in thermal ALD Al_2O_3 on GeO_x/Ge MOSCAPs [14], [15] is much higher as compared to that in plasma-enhanced ALD (PE-ALD) Al_2O_3 on GeO_x/Ge MOSCAPs [16]. We suspect that the reason for the discrepancy is that, unlike PE-ALD, thermal ALD requires water as a pre-cursor for oxygen. Since GeO_x is hygroscopic and thus, very susceptible to moisture, this might be a reason for the larger oxide charge trapping responsible for the hysteresis as a result of water exposure during thermal ALD. From the hysteresis, trapped oxide charge density (N_{ot}) can be extracted using [12]

$$N_{ot} = \frac{\Delta V_{FB} C_{ox}}{q}, \tag{1}$$

where ΔV_{FB} is the V_{FB} shift (also known as hysteresis) between the bidirectional 100 kHz C-V sweep, q is the elementary charge, and C_{ox} is the oxide capacitance per unit area, which was calculated to be $1.4\mu F/cm^2$ using the Maserjian *et al.* method [17] accounting for quantization effects, corresponding to an EOT of 2.5 nm. From eq. 1, N_{ot} of 4.25×10^{12} cm^{-2} and 1.21×10^{12} cm^{-2} was

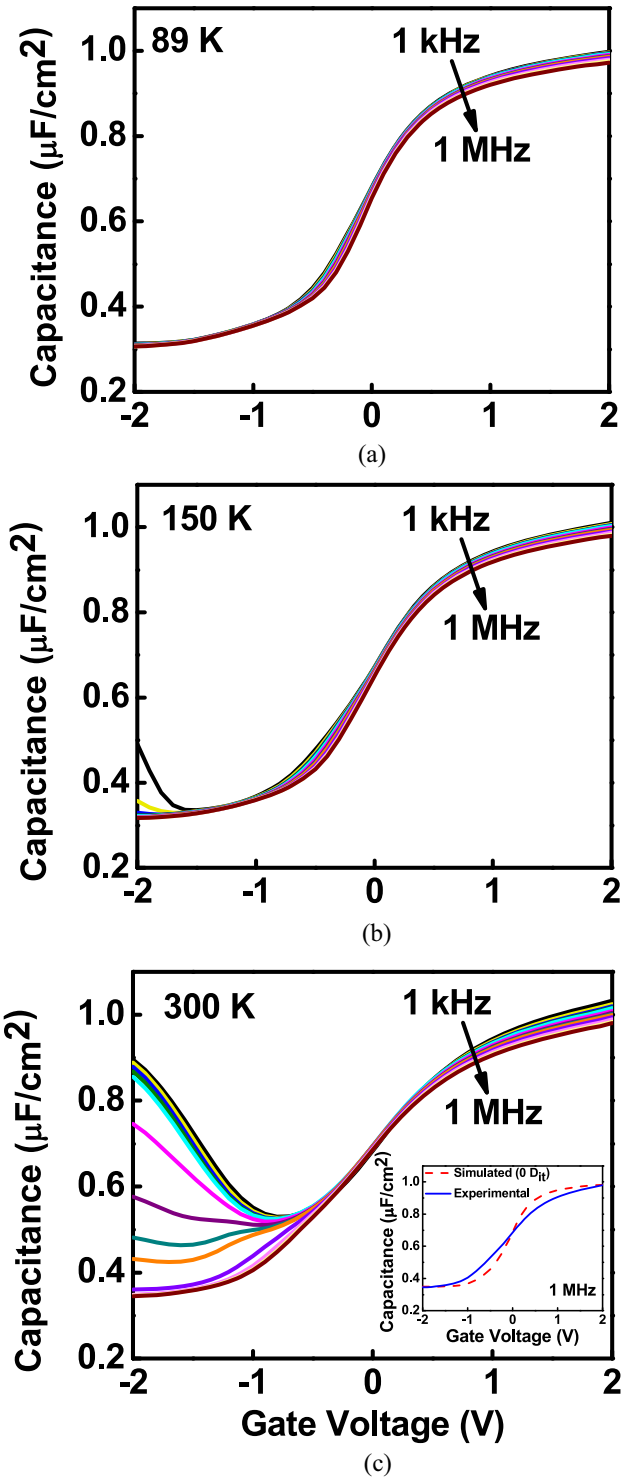

FIGURE 5. ***C-V*** **characteristics of the Al/Al_2O_3/GeO_x/Ge MOS-C on Si via a composite AlAs/GaAs buffer architecture at (a) 89 K, (b) 150 K, and (c) 300 K. (Inset) Comparison of 1 MHz simulated (with zero D_{it}) and experimental curve showing limited *C-V* stretch-out.**

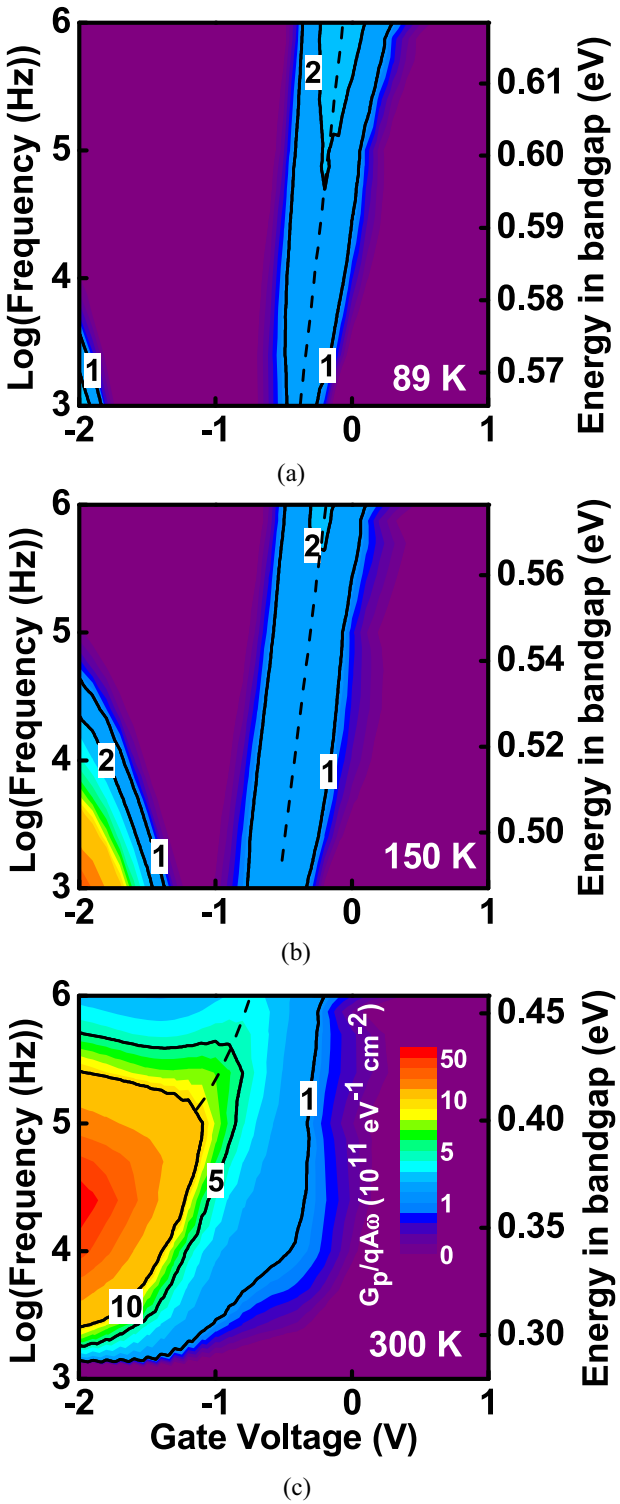

FIGURE 6. **Conductance (G_p/ω) contours of the Al/Al_2O_3/GeO_x/Ge MOS-C on Si via a composite AlAs/GaAs buffer architecture at (a) 89 K, (b) 150 K, and (c) 300 K. All figures follow the color scale shown in Fig. 3(c).**

extracted from 300 K and 89 K, respectively. Additionally, the MOS-Cs exhibited limited C-V stretch-out, as shown in the inset of Fig. 5(c), where a simulated 300 K 1 MHz curve with zero interface state density (D_{it}) is shown compared to the experimental 300 K 1 MHz curve. The parameters used for the simulated 1 MHz curve include a doping density of 1.24×10^{18} cm^{-3}, as estimated from the maximum-minimum capacitance technique [12]; N_{ot} of 4.25×10^{12} cm^{-2},

as extracted earlier from the 300 K C-V data from eq. 1; and D_{it} of 0 cm^{-2} eV^{-1} uniformly distributed throughout the bandgap. Limited C-V stretch-out of the experimental C-V curve as compared to the simulated C-V curve is indicative of low interface states throughout the upper half of the Ge bandgap [18]. The MOS-C's also demonstrate low frequency dispersion in the accumulation regime of 1.80% per decade over three decades at 300 K, which reduces down to 0.87% per decade over three decades at 89 K. The low frequency dispersion of the MOS-C's at 300 K suggests low interface states near midgap [18]. We speculate that this reduction in frequency dispersion is a reflection of the weak temperature dependence of the supply of carriers to the accumulation layer. Suggestive of low interface states near the conduction band edge is a low frequency-dependent V_{FB} shift [18], [19], which was calculated to be 59 mV, 77 mV, and 153 mV for 89 K, 150 K, and 300 K C-V measurements, respectively. Finally, there is an apparent small frequency dispersion kink in the depletion regime due to interfacial traps, as observed clearly in Fig. 5(a) and (b).

Fig. 6(a)–(c) shows the conductance contours corresponding to G-V sweeps measured at (a) 89 K, (b) 150 K, and (c) 300 K, respectively, which demonstrates the Fermi level efficiency (*FLE*) of the MOS-Cs. The Fermi level trace (dotted black line) at each measurement temperature follows the conductance peaks under different frequency and bias conditions. Efficient biasing of the Fermi level from near midgap to close to the conduction band edge is observed in the MOS-C, as demonstrated by the steepness of the Fermi level traces with respect to gate bias change. Quantitative calculation of the *FLE* [20] was performed using

$$FLE = \ln\left(\frac{f_2}{f_1}\right)\frac{[kT/q]}{(V_1 - V_2)}\%, \tag{2}$$

where f_1 and f_2 are the frequencies at which the depletion regime G_p/ω peaks occur under bias V_1 and V_2, respectively, k is the Boltzmann constant, T is temperature, and q is the elementary charge. Shockley–Read–Hall statistics can be applied to demonstrate *FLE* as a function of energy within the Ge bandgap using [21]

$$\tau_n = \frac{1}{2\pi f} = \frac{1}{\sigma_n v_{th} n_i}\exp\left(-\frac{E_t - E_i}{kT}\right), \tag{3}$$

where τ_n is the time constant for electrons, f is the measurement frequency, σ_n is the electron capture cross section, v_{th} is the thermal velocity of electrons, n_i is the intrinsic carrier concentration of Ge, E_t is the trap energy level, E_i is the midgap energy level, k is the Boltzmann's constant, and T is temperature. σ_n was assumed to be a constant value [13] of $10^{-16}cm^{-2}$ [22]. Fig. 7 shows the FLE of the MOS-C as a function of E_t away from E_i, where E_C is the conduction band edge of Ge. A peak FLE of 27.5% was observed 0.19 eV away from E_i, which demonstrates good modulation of the Fermi level with respect to gate voltage, suggesting low D_{it} throughout the bandgap. The poor *FLE* closer to E_i, which is partially attributable to the additional conductance contribution by the minority carrier response [8], is clearly demonstrated by the horizontal "arcing" of the Fermi level trace, which can be clearly seen in Fig. 6(c). Conductance contours extracted from G-V measurements performed at various temperatures from 89 K - 300 K were utilized in the extraction of *FLE*, as each temperature allows the sampling of a limited region of the Ge bandgap, as shown in the inset of Fig. 7.

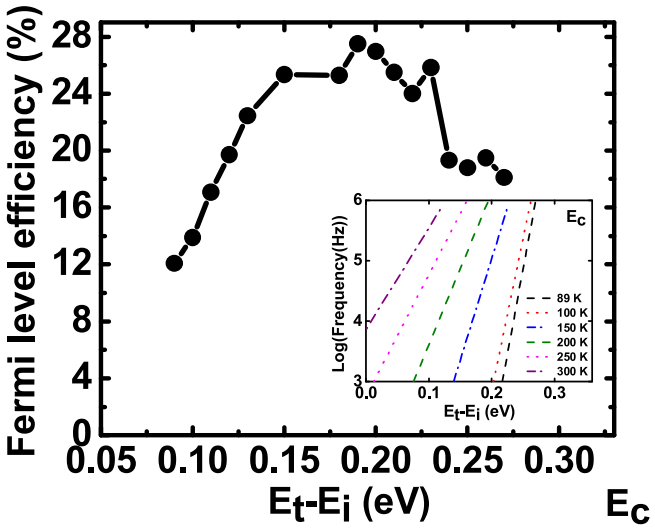

FIGURE 7. FLE as a function of energy of the Al/Al_2O_3/GeO_x/Ge MOS capacitor on Si via a composite AlAs/GaAs buffer architecture. (Inset) Ge bandgap energy ranges accessible at various measurement temperatures (89–300 K).

E. MOS CAPACITOR D_{IT} DISTRIBUTION

D_{it} was extracted from the conductance method with surface potential fluctuation correction [23], [24] using

$$D_{it} = \left(\frac{G_p}{\omega}\right)_{\max}\left[f_D(\sigma_s)\, qA\right]^{-1}, \tag{4}$$

where $(G_p/\omega)_{\max}$ is the maximum parallel conductance G_p normalized by angular frequency ω, q is the charge, $f_D(\sigma_s)$ is the universal function of the standard deviation of band bending σ_s, and A is the capacitor area. The conductance method was performed from 89 K-300 K to allow sampling of the D_{it} distribution at various ranges of the bandgap, where eq. 5 can be applied to show the distribution of D_{it} as a function of energy within the Ge bandgap. $f_D(\sigma_s)$ is determined by fitting the approximate width of the conductance (G_p/ω) plot to established metrics, as discussed in [23]. Fig. 8 shows the extracted D_{it} as a function of $E_t - E_i$. A peak D_{it} of 1.09×10^{12} cm^{-2} ev^{-1} was observed close to the conduction band edge, E_C, while a minimum D_{it} of 8.55×10^{11} cm^{-2} eV^{-1} was observed approximately 0.15 eV away from E_C. Moreover, the D_{it} numbers are consistent with the *FLE* calculations, with higher D_{it} being responsible for Fermi level pinning, and therefore a lower *FLE*.

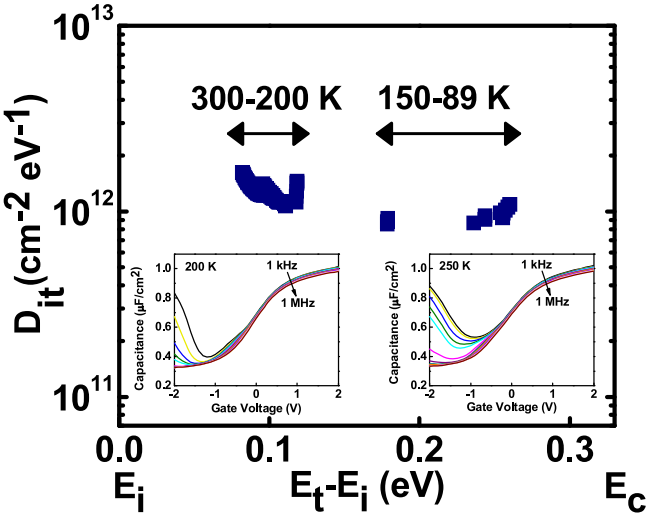

FIGURE 8. D_{it} **as a function of energy of the Al/Al_2O_3/GeO_x/Ge MOS capacitor on Si via a composite AlAs/GaAs buffer architecture. (Insets)** *C-V* **measurement of the device at 200 and 250 K, showing inversion response.**

Furthermore, the correlation between the extracted D_{it} and *FLE* are consistent with correlations reported elsewhere [19], [25]. The extracted D_{it} numbers are comparable to some of the values reported for the state-of-the-art bulk Ge MOS devices [26], which suggests both excellent passivation of the Ge surface as well as a defect-minimal Ge epitaxy on Si. The higher D_{it} extracted from the 200 K - 300 K measurements reflect an upper bound due to the temperature-dependent supply of minority carriers to the inversion layer which contribute to higher conductance, and thus lead to an overestimation of D_{it} [13], [22]. The insets of Fig. 8 show the inversion response of the device at both 200 and 250 K, which is due to the minority carrier response. The inversion response is also apparent from C-V measurements at 300 K, as shown in Fig. 5(c).

IV. CONCLUSION

In summary, high-quality epitaxial Ge was grown on composite large bandgap AlAs/GaAs buffer heterogeneously integrated on Si substrate. NMOS capacitors were fabricated from the aforementioned material stack for the first time. Distinct, well-defined Ge, AlAs, and GaAs peaks were observed from simulated and experimental [10] x-ray rocking curves. In addition, negligible interdiffusion of the underlying buffer into the epitaxial Ge, as confirmed by SIMS, EDS elemental mapping, and EDS line profile, further demonstrate the successful growth of a high-quality epitaxial Ge layer. The fabricated NMOS devices demonstrated excellent electrical characteristics with efficient modulation of the Fermi level from midgap to near the conduction band edge and a peak *FLE* of 27.5% corresponding to the low D_{it} value of 8.55×10^{11} cm^{-2} ev^{-1} Moreover, 300 K frequency dispersion was found to be as low as 1.80% per decade and a low frequency-dependent V_{FB} shift of 153 mV was observed, confirming low D_{it} near the conductance band edge. Furthermore, limited C-V stretch-out was observed confirming low D_{it} throughout the upper half of the Ge bandgap. The high-quality growth of epitaxial Ge on AlAs/GaAs buffer heterogeneously integrated on Si substrate and the superior electrical characteristics of the heterogeneously integrated Ge NMOS devices suggest the viability of future high-mobility channel material integration on Si *via* large bandgap buffer architectures for high-speed, low-voltage, high-performance CMOS logic applications.

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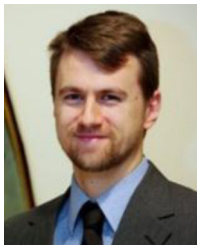

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