Electrical Characterization of Ruthenium Dioxide Schottky Contacts on GaN

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Thesis submitted to the faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

Master of Science
In
Electrical Engineering

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9 December 2014
Blacksburg, VA

Keywords: Schottky, GaN, Electrical Characterization, Ruthenium Dioxide, I-V

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Abstract

A film which is optically transparent and electrically conductive is difficult to come by but can be realized in ways such as doping an oxidized film or by oxidizing a metallic film resulting in what is known as a transparent conducting oxide (TCO). TCO's have many important uses in electronics, especially as the top contact in to solar cells where efficient transmission of light and low electrical resistivity allow for higher efficiency solar cells and as the gate contact in AlGaN/GaN HFET's allowing for optical characterization of the subsurface transistor properties. Because these devices rely heavily on the characteristics of its material interfaces, a detailed analysis should be done to investigate the electrical effects of implementing a TCO.

In this work, the electrical characterization of ruthenium dioxide (RuO_2) Schottky contacts to gallium nitride (GaN) formed by evaporating ruthenium with a subsequent open-air annealing is presented. The results gathered from the current-voltage-temperature and the capacitance-voltage relationships were compared to ruthenium (Ru) on GaN and platinum (Pt) on GaN. Additionally, the measurement and analysis procedure was qualified on a similar structure of nickel on GaAs due to its well-behave nature and presence in the literature. The results indicate that an inhomogeneous Gaussian distribution of barrier heights exists at the RuO_2/GaN interface with an increase of 83meV in the mean barrier height when compared to Ru/GaN.

Acknowledgements

The author would like to give thanks to the following people for their contribution to this research. I would like to thank my research advisor, Dr. Louis Guido for his guidance and input into much of this research. Additionally, I would like to thank Dr. G.Q. Lu and Dr. Alex Aning for their input and guidance in completing this thesis. I would like to thank my colleagues Kevin Chern, Tim Ciarkowski, and Eric Carlson for their input and hands-on help in the labs. Finally, I would like to thank my parents for their unconditional support that has allowed me to reach my potential.

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1 Introduction

III-nitride based semiconductors such as aluminum nitride (AlN), gallium nitride (GaN), and indium nitride (InN) have been known for their exceptional electrical, optical and thermal properties. These materials have proven their usefulness in areas such as high-speed electronics, power electronics, and optoelectronics. As a result of the large bandgap, III-nitride semiconductors have low intrinsic carrier concentrations, high saturation-electron drive velocity and high breakdown fields. The bandgap can also be tightly controlled between 0.7 eV for InN to 6.2 eV for AlN with good lattice matching making it ideal for complex optoelectronic devices. These semiconductors have shown good thermal and radiation resistant properties. Although there is still work to be done on maximizing the potential of III-nitride semiconductors, the promise they show in replacing current state-of-the art devices has attracted a lot of attention.

In GaN Heterojunction Field Effect Transistors (HFET) one of the most important interfaces is the gate metal to semiconductor junction. In an HFET this is normally a Schottky barrier structure used to modulate the 2-dimensional electron gas (2DEG) below the surface effectively switching the transistor on and off. A Schottky barrier is the unique effect that occurs when a metal is placed in intimate contact with a semiconductor whose electron affinity is smaller than the metal work function. A rearrangement of charge on the surface of the semiconductor creates an energy barrier at the metal-semiconductor (MS) junction leading to rectification in the current voltage characteristics. Because GaN HFET's are normally-on devices a Schottky gate with minimum leakage current is necessary. This makes characterization of both the metal material and interface with the semiconductor critical to obtain the best switching characteristics of the transistor.

The transparent conductive oxide (TCO), Ruthenium dioxide, has proven to be a good candidate for Schottky contacts to GaN due to its larger work function (>5eV), high electrical conductivity (~40μΩ·cm), and good thermal stability. Additionally, ruthenium dioxide is optically transparent introducing the possibility of optically characterizing the interface and subsurface properties in GaN HFETs. These characteristics make RuO_2 an exciting material to study. In this work the author electrically characterizes RuO_2 Schottky barriers fabricated on n-type GaN. The results of this experiment are compared to an un-annealed ruthenium Schottky contact sample along with the widely used platinum Schottky contact to GaN. In addition to qualifying the results of this experiment, the evaluation technique was first attempted on the well behaved nickel Schottky contact to GaAs to ensure validity of the approach.

2 Literature Review

2.1 Properties of III-Nitrides

The III-Nitride semiconductor group consists of Aluminum Nitride, Gallium Nitride and Indium Nitride and has been considered a promising material system for applications in light emitting/detecting devices and in high power electronics. The unique properties of some of these semiconductors such as Gallium Nitride also appeal as devices requiring normal operation at high temperatures and in the presence of radiation [1, 2]. One of the reasons there has been a large push for research on III-Nitrides is because of the well-controlled bandgap both below and well above the visible field. This allows for tightly controlled emitters and detectors that can operate from deep ultraviolet to far infrared. The comparison of bandgap with other semiconductors is seen in Figure 1.

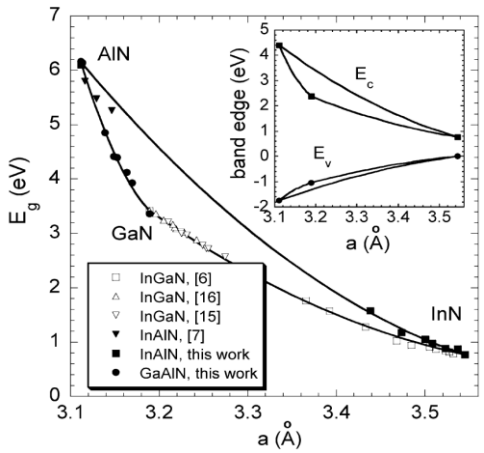

Figure 1. Band gap of various semiconductors. Notice that by changing the makeup of the III-Nitride semiconductors you can modulate the bandgap greatly [3]

2.1.1 Crystal Properties

Unlike the other III-V semiconductors the III-Nitride semiconductors typically crystalize in the wurtzite (Wz) phase [4]. The wurtzite structure belongs to the hexagonal crystal structure and in the case of III-nitrides consists of tetrahedrally coordinated nitrogen atoms along with the respective column three atom. Each unit cell comprises of 6 atoms of the two types thus requires two lattice constants, 'c' and 'a'. The unit cell is made up of two close-packed planes each with two types of atoms stacked in the [0001] direction. Because each plane consists of two types of atoms the stacking sequence becomes AaBbAa. [5]

Although III-nitrides tend to crystallize in the wurtzite structure (as seen in Figure 2), these semiconductors can be forced into the zincblende and rock salt crystals. In the case of the zincblende structure, the tendency to relax into the wurtzite phase is overcome due to the surface structure of the substrate. This was first discovered by Mizuta et al [6] when GaN was grown at low temperatures on a (100) oriented GaAs substrate. It has also been shown that III-nitrides can be grown in zincblende on Si[7], SiC[8], MgO[9] and on (0001) oriented sapphire[10] substrates. Zincblende shows a smaller bandgap, higher electron saturation drift velocity and freedom from spontaneous/piezoelectric polarization.

However the inability to grow zincblende material void of defects leaves hexagonal GaN as the main focus of research.

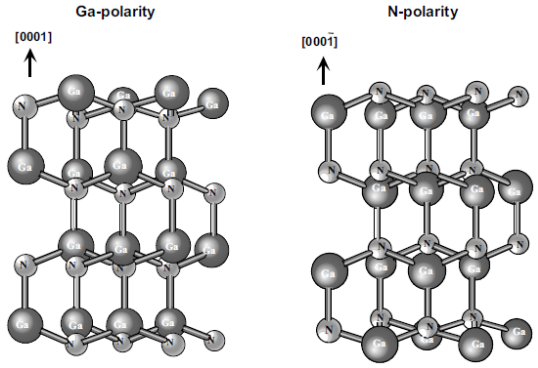

Figure 2. Stick and ball representation of the tetrahedrally coordinated GaN crystal. [5]

The rock salt structure can only be achieved by forcing the nitride and associated column three element to bond ionically instead of covalently. Thus, this structure cannot be achieved in larger quantities via epitaxial growth and typically requires a large amount of pressure applied by a device (20 GPa for AlN) such as a diamond anvil cell [11]. Because large quantities of III-nitrides in the rock salt crystal structure is difficult to fabricate, the use in electronic devices has not been well researched.

2.1.2 Electrical Properties

III-nitrides are heavily studied not only because of their favorable material properties but also because of their electrical properties. These semiconductors have become the standard in optoelectronics, high frequency switching applications and high power devices. A comparison of different electrical properties of III-V semiconductors is given in Table 1.

Table 1. Table showing electrical characteristics of III-nitrides and various semiconductors [12, 13]

Electrical Properties at 300K (WZ)	GaN	AlN	InN	Si	GaAs	3C-SiC	4H-SiC	6H-SiC
Band Gap (eV)	3.44	6.13	0.7	1.124 (Γ/Δ)	1.424	2.36 (ΓX)	3.23	3.0
Direct/Indirect Band Gap	Direct	Direct	Direct	Indirect	Direct	Indirect	Indirect	Indirect
Dielectric Constant	10.4	9.14	8.4	11.97	12.80	9.52	6.5	9.66
Electron Effective Mass (m_0)	0.22	0.3	0.11	0.191	0.063	$0.65_l/0.25_t$	$0.29_l/0.42_t$	$2.0_l/0.42_t$
Breakdown Field (V/cm)	$5 \cdot 10^6$	$(1.2\ to\ 1.8) \cdot 10^6$	-	$3 \cdot 10^5$	$4 \cdot 10^5$	10^6	$(3\ to\ 5) \cdot 10^6$	$(3\ to\ 5) \cdot 10^6$
Electron Mobility (cm^2/Vs)	900	300	250	1450	9000	510	948	480
Intrinsic Carrier Concentration (cm^{-3})	Between $5 \cdot 10^{19}$ and $5 \cdot 10^{16}$	$2.47 \cdot 10^{-32}$	$1.34 \cdot 10^{13}$	$1.02 \cdot 10^{10}$	$2.1 \cdot 10^6$	0.39	$2.92 \cdot 10^{-8}$	$1.92 \cdot 10^{-4}$

The unique electrical characteristics of III-nitrides have played a huge role in furthering the technological advancement in both power and high frequency electronics. In these fields it's the materials limitations that define the range of operation in which an ideal device can be pushed. In power electronics, one of the limiting factors of devices is the breakdown electric field which dictates both the size and the voltage range that a device can safely operate. Materials with larger bandgaps, such as in the case of GaN and AlN, are able to sustain high electric fields before breaking down. The intrinsic carrier

concentration and its dependence on temperature also play a larger role in power electronics. At elevated temperatures, the device can no longer operate once the intrinsic carrier concentration becomes comparable to the doping. III-nitrides also have favorable characteristics in terms of electron mobility and saturation velocity which make them ideal in high frequency switching applications.

2.1.3 Optical Properties

Optical applications for III-nitrides span a wide variety of devices, including visible range diode lasers, LED's, solar cells and photodetectors. III-nitrides became a very good candidate for optoelectronics because of their large bandgap sizes and direct bandgaps [14]. Also, the binary alloys GaN, AlN, and InN can be grown in different concentrations so that bandgaps between 6.13eV and 0.7eV can be created, giving them the ability to emit/detect wavelengths of light between 202nm to 1771nm.

The first fabricated LED was documented in 1907 when Round [15] discovered that various color light could be emitted from a SiC crystal at voltage biases as small as 10 volts. The nitride semiconductor material system wasn't looked at until it was realized that, if implemented properly, they could be used to emit light in the UV range. Although, the first LED was documented in 1907, it wasn't until 1971 that electroluminescence was proven in GaN [16]. One of the reasons why the development of III-nitride optical devices took this long was because of the difficulty in fabricating high quality crystalline samples. When GaN was grown, it was naturally n-type material and took a great deal of effort to p-type dope it high enough to counteract the intrinsic carriers. In fact, these problems still exists today and will be addressed in a later section.

2.2 Growth of III-Nitrides

[5] The growth of quality III-nitride semiconductors has been in development for more than 50 years and still requires work to compete with its silicon counterpart. It has been said that the current state of growth techniques can be contributed to a handful of breakthroughs including, the first synthesis of AlN [17], GaN [18] and InN [19], the first electronics-grade epitaxial deposition of GaN [20], the incorporation of a buffer layer [21, 22], and finally the successfully p-type doping of GaN [23]. The three main methods that have traditionally been used to grow III-nitride crystalline material include hydride vapor phase epitaxy (HVPE), organometallic vapor phase epitaxy (OMVPE), and molecular beam epitaxy (MVE). These methods and the materials required to fabricate these crystals are covered in the following sections.

2.2.1 Methods

Because no cost efficient native substrates exist for use in III-nitride growth like it does for standard semiconductors, vapor phase epitaxy (VPE) has been favored as the primary means of depositing GaN, AlN and InN. VPE consists of taking a carefully chosen substrate and exposing it to one or more reactive gases. Once the two come into contact, the gases decompose on the substrate in an epitaxial fashion thereby allowing crystalline films of controlled thickness to be deposited. There exist many types of VPE all of which are referred to by the type of source gas used for deposition. For example, if a source containing the column V element nitrogen and a hydride (such as in the case of ammonia, NH_3) is flowed over the column III melt, the process is termed hydride vapor phase epitaxy (HVPE). Additionally, two gasses can be combined where one is an organic compound containing a column III element. This process

is referred to as organometallic vapor phase epitaxy (OMVPE) or metalorganic chemical vapor deposition (MOCVD). HVPE is popular for use in depositing thicker layers, large enough to delaminate from the substrate for use as a self-supporting sample. OMVPE has shown to produce higher quality films and abrupt heterojunctions and thus has become the most widely used growth technique for optoelectronic devices. A mixture of these two methods has also shown to decrease the defect density of films through the use of a buffer layer in what is known as a two-step process. Both HVPE and OMVPE along with the two-step process are discussed in the following sections [5].

2.2.1.1 Hydride Vapor Phase Epitaxy

HVPE has become one of the major methods of growing III-V semiconductors after the development of halide precursor techniques were applied to GaAs in the late 1960s. Extensive research was done on the development of HVPE growth conditions and substrate type for high growth rate but was almost phased out in the 1980s when it seemed impossible to create GaN films with low enough defect densities to allow p-type doping. It wasn't until the two-step growth process originally developed for OMVPE was applied to HVPE along with a successful p-type doping method that HVPE became more popular [24].

A precursor is required for each element in the III-nitride material system to assist in the deposition on a substrate. In the case of GaN, the gallium precursor is created by flowing hydrogen chloride gas over a gallium melt to create $GaCl$. The possible reactions are shown below:

$$2Ga_{liq} + 2HCl_{gas} \leftrightarrow 2GaCl_g + 2H_{2_{gas}} \quad \textbf{(1)}$$

$$GaCl_{gas} + 2HCl_{gas} \leftrightarrow GaCl_{3_{gas}} + H_{2_{gas}} \quad \textbf{(2)}$$

Next, the group V precursor, ammonia in the case of GaN, is fed into the chamber using a separate line so that the mixing with the column III precursor can be properly contained. Inside the chamber, the gasses are combined in the mixing region of the tool and then the products of the reactions are expelled into the substrate region of the tool. The two possible mixing reactions are shown below [24]:

$$GaCl_{gas} + NH_{3_{gas}} \leftrightarrow GaN + HCl_{gas} + H_{2_{gas}} \quad \textbf{(3)}$$

$$3GaCl_{gas} + 2NH_{3_{gas}} \leftrightarrow 2GaN + GaCl_{3_{gas}} + 3H_{2_{gas}} \quad \textbf{(4)}$$

As with any system, there exist many variables that control the quality and growth rate of HVPE grown semiconductors. To minimize the contribution of the chamber during growth, the walls are elevated in temperature and made of a non-reactive material such as high purity quartz. Additionally, the gasses used to transport III-V are incredibly pure with values better than 7N (99.999% pure) for column III precursors and better than 5N (99.999% pure) for column V precursors [25]. Additionally, studies have been done to correlate the flow rate [26-28], carrier gasses [29, 30], growth temperature [27, 28], and buffer structures [31-33] to quality and growth rate but it was found that reactor geometry played the biggest role [25, 34, 35].

2.2.1.2 Organometallic Vapor Phase Epitaxy

Although the discovery of OMVPE has been disputed, most credit has been given to the first published technical article by Manasevits [36]. Manasevits showed that the growth of single crystal Gallium-V films could be grown on GaAs by mixing an organic gallium compound (triethylgallium or

trimethlygallium) with the respective group V hydride and transmitting the vapors to the deposition chamber. Because two methods for creating single crystalline III-V semiconductors existed both of which could be scaled for industrial use, the popularity was determined by the quality of material produced in each method. It was the exhibition of high purity GaAs using OMVPE [37] and its success in minority carrier devices such as LED's [38], solars cells [39], photocathodes [40] and lasers [41] that ultimately lead to the decline in popularity of HVPE and increase in the industrial use of OMVPE for III-V semiconductor growth. Additionally, the OMVPE method has been shown to produce almost atomically abrupt junctions of quality comparable to the MBE process [42].

As stated earlier, if one or more metalorganic liquids are used the process is termed organometallic or metalorganic vapor-phase epitaxy. Typically the metal organic solutions are liquid at room temperature thus allowing a carrier gas to be bubbled through them. The resultant vapors are mixed and transported to the deposition chamber. The OMVPE process requires a pyrolytic process to decompose and deposit epitaxially on the surface of the substrate, therefore the substrate is heated while the walls of the reactor are chilled. This maximizes the decomposition flux at the surface of the substrate while minimizing the growth on the walls of the reactor.

As with HVPE, OMVPE is a complicated process made simpler with the examination of macroscopic growth effects due to the variation of growth parameters. Initially, the growth process was treated as an art where knobs and buttons were tweaked until quality film was produced. This is because originally the growth process was not well understood until examination of the dependence on growth parameters uncovered the fundamental growth process. Upon variation of the growth temperature it was found that the rate of growth increased at low temperatures, peaked and then began to decrease with high temperature. It was then determined that the process was kinetically and thermodynamically limited at low and high temperatures respectively. Next, it was found that the peak was modulated through the variation of gas velocity, indicating this region was limited by the rate of precursor arrival to the substrate (also known as mass transport limited). Thus, to optimize the growth rate, the substrate must be held at temperatures where the process is mass-transfer limited instead of thermodynamically or kinetically limited. The Arrhenius plot below shows each growth-limiting regime [42].

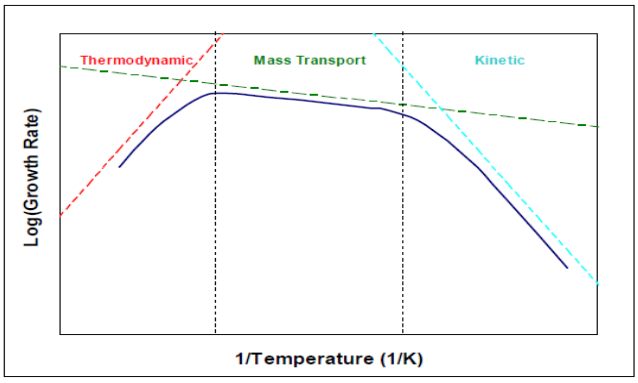

Figure 3. Arrhenius plot showing the three limiting regimes of an exothermic growth such as in the case of OMVPE [42]

Typical organometallic precursors for III-nitride growth include trimethylgallium (TMGa-$(CH_3)_3Ga$), trimethylindium (TMIn-$(CH_3)_3In$), and trimethylaluminum (TMAl-$(CH_3)_3Al$) with ammonia as the nitride precursor [43]. In the case of III-nitride growth, ammonia is very thermally stable this a very high temperature on the order of 550°C for In and 1000°C must be reached before quality crystalline films can be achieved. The heat required to facilitate the reduction of the ammonia molecule in conjunction with high nitrogen vapor pressure causes loss of nitrogen at the surface of the film. Thus the V/III precursor flow ratio is very large to prevent large densities of nitrogen vacancies.

2.2.1.3 Buffer Layer

As mentioned previously, no native substrates exist for the epitaxial growth of II-nitrides so a foreign substrate of desired crystal structure and similar lattice constants is required. This lattice mismatch causes defects at the film/substrate boundary that can propagate vertically through the film, as seen in Figure 4. These defects manifest themselves as wide X-ray rocking curves, rough surfaces, high electron concentrations (up to $10^{19}\ cm^{-3}$), and a luminescesce spectra with a considerable yellow emission. One successful defect engineering technique consists of growing a buffer layer designed to be lattice matched to the film. The number of dislocations at the surface of the buffer layer decreased as the buffer layer thickness was increased as seen in Figure 4. The surface of the buffer layer can then act as a highly lattice matched substrate for higher quality grown films via epitaxy. Annealing the buffer layer immediately after its growth has also been shown to contribute to the reductions of dislocation densities. However, the defect density will saturate with increased time making longer annealing times useless. In the case of GaN, electron concentrations of hexagonally grown films deposited directly on sapphire could approach $10^{20}\ cm^{-3}$ while the implementation of a buffer layer could bring the concentrations within the non-degenerate region with concentrations around $10^{17}\ cm^{-3}$ [5].

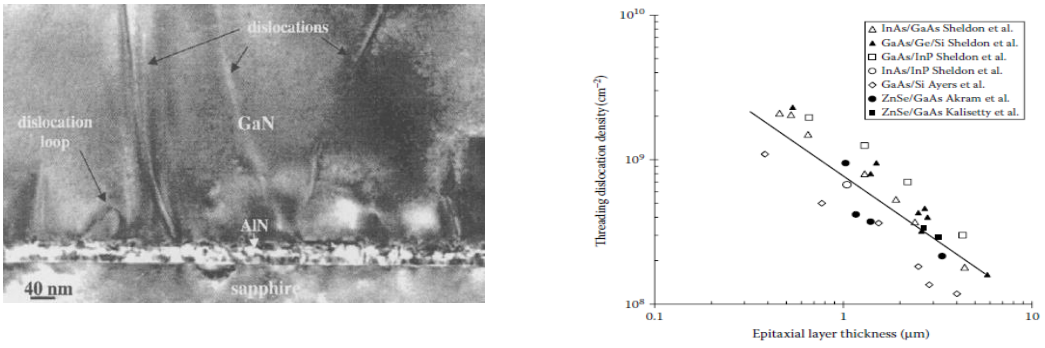

Figure 4. The threading dislocation density vs. thickness of grown buffer layer from [43]

2.2.2 Substrates

III-nitride device development has been greatly impeded by the inability to grow nearly perfect crystal material which translates into materials with large intrinsic carrier concentrations, surface defects, and poor physical properties at the substrate/film barrier. Because III-nitrides currently have no readily available native substrates, an epitaxial process on a latticed matched and thermally matched substrate is required to get the highest quality material. The overall density of defects and the compatibility of a film with the substrate depends on the thermal expansion, the lattice constant, and chemical compatibility between the two material systems [44]. If the thermal expansion between the film and

substrate is too large then, during cooling, the semiconductor film will crack and separate. Additionally, a film needs to be carefully matched to the crystal structure and lattice constant of a substrate. In the case of GaN, depending on the crystallinity of the substrate, it can be grown zinc-blende or in the wurtzite crystal structure [5]. This characteristic can be very useful since each structure has its own unique properties. For example the wurtzite phase has a larger bandgap than the zincblende structure and shows a larger piezoelectric polarization. On the other hand the zincblende structure has a much smaller piezoelectric polarization when strained which is useful in optoelectric applications. Finally, the chemical compatibility between the two materials needs to be ideal so that the growth process can begin.

Dislocations in a semiconductor can cause a lot of problems not only affecting the physical properties of the material but also affecting the electrical properties. Although lattice mismatched substrates can be used to grow film, they introduce threading dislocations on the order of 10^8 to $10^{10}\ cm^{-2}$ which start at the substrate/film boundary and propagate to the surface of the film. A threading dislocation provides a path for impurities to diffuse directly into the semiconductor which in turn can create a highly conductive vertical path while impeding transport horizontally. In optical devices this manifests itself as a larger dark current in detectors and lower quantum efficiency in emitters and in the case of electrical devices these dislocations can cause higher gate leakage current and output conductance's [5].

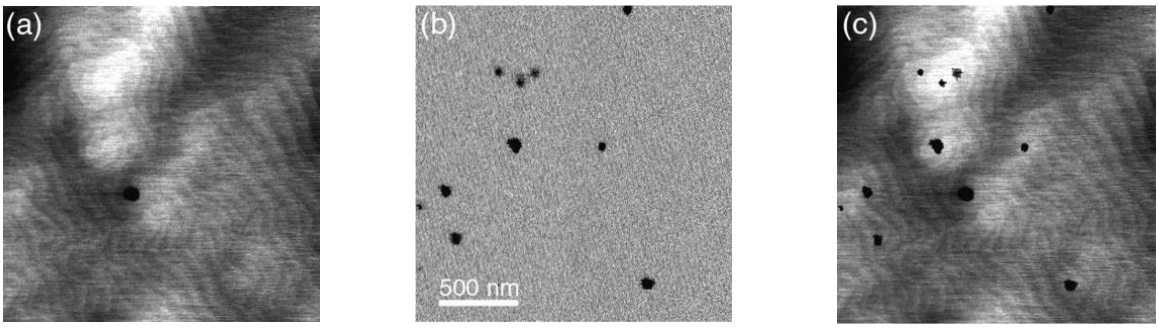

Figure 5. A scanning current-voltage microscopy (SIVM) measurement on an MBE grown GaN film. (a) is a topographical image of the substrate showing the spiral hillocks typically seen in MBE grown films. A current map (b) was done in the same region where the darker regions show current above the $4{\cdot}10^{-13}$ A limit (black regions represent ~$2{\cdot}10^{-11}$ A). In (c) the topography is overlaid on the current topography [45].

Sapphire substrates are typically used to grow III-nitrides because of its low electrical conductivity and high thermal conductivity making it ideal as a platform for power devices. Also, the cost of sapphire substrates is substantially lower than other options such as SiC. III-nitrides have traditionally been on sapphire substrates oriented with a (0001) surface structure but growth has also been reported on the $(21\bar{3}1)$, $(110\bar{1})$, $(1\bar{1}02)$, and the $(11\bar{2}0)$ surfaces. Growth has also been presented on Si, NaCl, GaP, InP, SiC, W, ZnO, $MgAl_2O_4$, TiO_2, and MgO substrates [5]. Table 2 lists the Properties for common substrates used in epitaxial III-nitride growth.

Table 2. List of common substrates for III-nitride epitaxial growth and their properties [13]

	Sapphire	GaN	GaN	Si	4H-SiC	6H-SiC	ZnO
Crystal Structure	rhombohedral	hexagonal	zincblende	diamond	Hexagonal	Hexagonal	hexagonal
a_0 (Å)	4.758	3.189	4.52	5.431	3.07	3.08	3.2496
c_o (Å)	12.991	5.186	-	-	10.05	15.12	5.2065
Thermal Conductivity (W/cm·K)	0.3-0.5	1.3	1.3	1.3	3.7	4.9	0.3-0.4
Thermal Expansion ($°C^{-1}10^{-6}$)	8.3	$5.59_a/3.17_c$	4.59 [46]	2.6	-	4.3	-
Bandgap (eV)	9.9	3.39	3.2	1.12	3.23	3.0	-
Mismatch w/ GaN	+49.2%	0%	-	-	3.63%	3.36%	+1.9%

2.2.3 Doping

A requirement for electronic devices is the use of finely controlled doping to modulate the Fermi level throughout a bulk semiconductor. In GaN typical n-type dopants include C, Si, and Ge sitting on Ga sites or Se on N sites which act as donors. P-type dopants in GaN include Be, Mg, Ca, Zn, and Cd on Ga sites and C, Si, and Ge on Ga sites. In the case of impurities, a low ionization energy and low formation energy is required to have a high probability of incorporating said dopant. C_{Ga}, Si_{Ga}, and Ge_{Ga}, have ionizations energies of 34.0, 30.8, and 31.1 meV respectively and formation energies of 5.7-6.5, 0.9, and 2.3 eV in Ga-rich conditions respectively. Thus, Si_{Ga} is best suited for n-type doping. For acceptor impurities Be_{Ga} and Mg_{Ga} have been determined as the best candidates for acceptor impurities however, because Be is a smaller atom, the ability for it to replace Ga and sit in interstitial sites creates a double donor. This makes Mg the favorable impurity for p-type doping.

Typically one of the biggest challenges in GaN based device development is the seemingly insurmountable n-type background carrier concentration. As stated previously, early unintentional electron concentrations ranged anywhere between 10^{18} and 10^{20} cm^{-3} making the creation of p-type material seem impossible. Any effort effectively compensated the high electron concentrations creating a highly resistive film. Early attempts at using Mg failed primarily for two reasons, the inclusion of hydrogen (ammonia precursor) passivated the Mg atoms and heavily Mg-doped GaN can induced self-compensation through the inclusion of donor defects. It was later found during the cathodoluminescence of Mg-doped GaN that a low energy electron beam irradiation treatment caused the H-Mg molecules to dissociate allowing the hydrogen atom to diffuse to the surface and reacts with an ambient gas such as N_2. Additionally, this process can be mimicked through the use of a high temperature annealing at temperatures in excess of 600°C or by UV illumination at temperatures above 500°C. [5]

2.3 Schottky Contacts

2.3.1 Background

The discovery of the first rectifying contact has been attributed to Ferdinand Braun during his attempts to use metal contacts on a semiconductor for electrolysis on the study of minerals in 1874. It was realized that as the polarity of voltage on this point contact rectifier was changed, the resistance would drastically increase or decrease accordingly. This effect of rectification was not well understood until Wilson published his theory of charge transport in semiconductors and insulators [47]. It was 7 years later, in 1938, that the theory of rectification was explained independently by three scientist, Davydov [48], Mott [49], and Schottky [50] however it was Mott that correctly predicted the direction of rectification. Although Mott derived the diffusion and drift currents of the majority carrier, his theory was

based on the principle that the space-charge region was absent of ions, making the electric field in this region constant. Motts' theory was later extended by Schottky and Spenke by substituting a semiconductor absent of donor ions with a semiconductor having spatially constant donor ions. This then corrected Motts initial theory of a constant electric field present in the space-charge region to one having a linearly decaying electric field. Schottkys' extension of Motts' theory predicted a barrier at the metal-semiconductor (MS) junction later known as a Schottky Barrier thus prematurely labeling metal-semiconductor rectifiers as Schottky Diodes. Although more developed, the Schottky-Mott rectification theory predicted the incorrect current limiting mechanism and current-voltage equation. In 1942 Hans Bethe made the most recent contribution to the metal-semiconductor diode model by correctly predicting thermionic emission to be the current limiting mechanism and thus deriving the current-voltage relationship that is used today.

2.3.2 Metal-Semiconductor Interface Models

2.3.2.1 Schottky-Mott Theory

To model the theoretical Schottky junction we can consider a non-interacting large work-function metal and n-type semiconductor whose surfaces are electrically identical to their bulk properties, Fig 1(a). If a conductive path is made between these two surfaces, electrons will flow from the semiconductor into the metal, thermal equilibrium will be reached and the two Fermi levels will line up, Fig 1(b). If the two surfaces are brought closer together, positive charge will begin to buildup on the semiconductor and negative charge on the metal so that thermal equilibrium is maintained, Fig 1(c). At a separation comparable to atomic spacing the electrostatic potential just outside of the metal and semiconductor becomes equivalent. From the figure below it's obvious that the barrier height as seen by electrons entering the semiconductor is $\phi_B = \phi_m - \chi_S$ [51, 52], where ϕ_m is the workfunction of the Schottky metal and χ_S is the electron affinity of the bulk semiconductor.

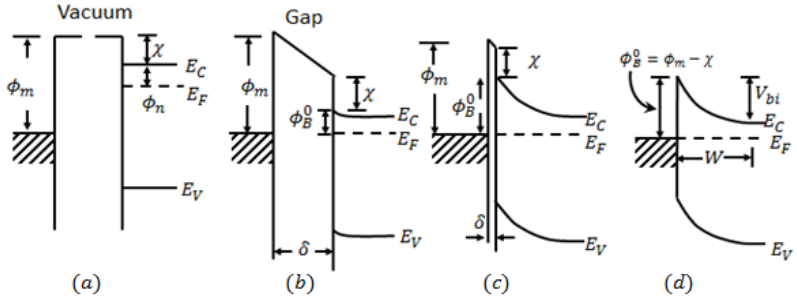

Figure 6. Energy band diagram of MS contact. When separated (a) the materials don't interact. Then as they are brought closer (b) the Fermi levels line up and the density of states at the semiconductor surface shift to compensate for the electric field. The gap is (c) and finally (d) becomes zero [51]. The last figure (e) shows an ideal SB with detailed energy levels labeled [53].

Accordingly, it is expected that the barrier height can be modulated linearly such that

$$S \equiv \frac{\partial \phi_B}{\partial \phi_m} = 1 \qquad (5)$$

also known as the Schottky-Mott limit. However, it has been shown experimentally that the barrier height is usually much less dependent on the metal work-function ($S < 1$). This phenomenon was first explained

as a coercion of the Fermi level in the semiconductor caused by some electric field at the interface. Bardeen first modeled this by assuming the field at the surface was due to either the termination of the crystal or the inclusion of impurities at the surface causing a charge-neutral level (E_0) in the bandgap. Sze and Cowley further developed this idea and derived the barrier height dependence with an atomic interfacial layer that is transparent to electrons with energy greater than the barrier height and charge density dependence on the semiconductor only. The equation takes the form of the following,

$$\phi_B = S(\phi_m - \chi) + (1 - S)\phi_{bno} \quad (6)$$

$$S = \left[1 + \frac{e^2 N \delta}{\varepsilon_0}\right]^{-1} \quad (7)$$

where ϕ_{bno} is the pinned barrier height, q is the charge of an electron, N is the density of charge in the interface at E_0, ε_0 is the permittivity of the interface layer, and δ is the thickness of the interfacial layer. Thus, the variation of the metal work-function is fully or partially negated by the screening of a thin charged interfacial layer at the MS junction [51].

2.3.2.2 MIGS

Early metal-semiconductor junctions were fabricated by pressing metal onto a semiconductor so that the probability of a thin oxide and impurity layer forming at the interface was high thus confirming Bardeens theory of an interfacial dipole layer. However, Heine noted that MS junctions fabricated by depositing metal vapors onto a freshly cleaved semiconductor plane still produced insensitive barrier height with respect to metal workfunction. This is also consistent by examining the effect of a vanishing interfacial layer thickness, δ, in the above equation for S [54].

Heine proposed instead that FLP was due to the probability of electron population just outside a metal surface vanishing exponentially inside of the semiconductor [54]. Although the probability of metal electrons spilling into the semiconductor decays exponentially, the magnitude is still great enough to screen the bulk charge neutral energy level (CNL) on the order of 10Å from the interface. The states at the interface were later referred to as metal induced gap states (MIGS) by Tersoff who improved model by calculating the pinning level (E_0) through the use of Green's function. His results showed that E_0 fell at the energy point where states in the forbidden gap transition from donor-like near the valence band to acceptor-like near the conduction band also known as the branch point energy. The model was shown to be in agreement with experimental results at the time [55]. Interestingly, this model can be related to Equations (6) and (7) by redefining the interfacial layer thickness, δ, as the penetration depth of the metal electron wavefunctions and the density, N, as the density of MIGS at the pinning energy E_0.

Exploiting the relationship between the product $\delta \cdot N$, the bandgap and the electronic contribution to the dielectric constant, ε_∞, Mönch showed that an equation for S depending solely on the material properties of the semiconductor could be successfully fit to experimental data. The slopes dependence on ε_∞ can be understood by noting that the depth and density of charge at the interface rely on the permittivity of electric fields in the semiconductor. Equation (8) effectively sets the theoretical barrier height of each semiconductor when only the MIGS interface model contributes to the pinning of the Fermi level in the interface and no second order inefficiencies exist.

$$S = [1 + 0.1(\varepsilon_\infty - 1)^2]^{-1} \quad \textbf{(8)}$$

2.3.2.3 UDM

Although the MIGS model supported the data, it did not explain metal-semiconductor barriers with a slope, S, different than that expected from the semiconductor electronic permittivity. Spicer et al. theorized that defects native to the semiconductor could pin the Fermi level especially in III-V semiconductors where atomic antisites could drastically change the donor or acceptor concentration at the surface. This paradigm became known as the unified defect model (UDM) [56].

Attempting to study the barrier height formation, Spicer et al. deposited various thicknesses of metal ranging from 0.001 ML (monolayer) to 10 ML onto a GaAs substrate. Using photoemission spectroscopy (PES) it was found that the Fermi level on n-type GaAs would decrease from the conduction band to a pinned level at around 0.75 eV from the valence band maximum (VBM) as the deposited atom increased from a 0 ML to 0.1 ML coverage. Likewise for a p-type sample, the Fermi level would increase from the valence band at 0 ML and pin at 0.5eV from the VBM upon reaching 0.1 ML atomic coverage. The unified defect model simply stated that a donor-like defect must be present in the band gap at 0.75eV from the VBM while an acceptor-like defect must exist at 0.5eV in from the VBM both of which must be induced by the deposition of atoms on the surface. Ga and As vacancies were thought to be the cause of pinning at these levels [57].

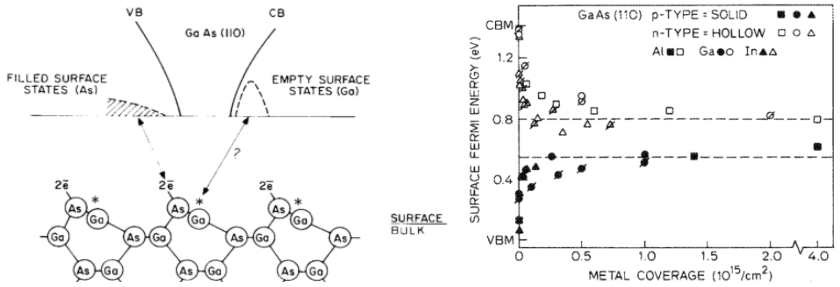

Figure 7. UDM predicted that surface defects states normally pasivated through surface reconstruction, as seen in A), could be brought back into the bandgap during metal deposition. In B) it can be seen that at very small surface densities of metal atoms, the surface Fermi level seems originate from either the valence band for p-type material or the conduction band for n-type material and pin at 0.5eV or 0.75eV from the valence band respectively [57].

The advanced unified density model (AUDM) expanded on the origin of these positions in GaAs. Since the surface of a cleaved GaAs plane could reconstruct itself to minimize dangling bond defects, it was theorized that the addition of deposited metal atoms on GaAs caused As antisites (As_{Ga}). The idea seemed solid since the ionization energies of the As_{Ga} double donors fall at 0.52 and 0.75eV with respect to the valence band however, it was later found that the deposited layers were actually unconnected islands and did not behave metallically. If deposition was instead done at low temperatures allowing for a uniform layer to be deposited the pinning level of both p- and n-type GaAs coincided with pinning due to the electronegativity of the metal [58].

2.3.2.4 DIGS

Utilizing photocapacitance transient spectroscopy (PCTS), Hasegawa and Ohno showed a pinning level dependence on the charge neutral level in not only metal-semiconductor (MS) interfaces but also semiconductor-semiconductor (SS) and insulator-semiconductor (IS) interfaces. Experiments were done on MIS structures. Results showed that the density of defect states (N_{SS}) at the surface of the semiconductor were U-shaped with a minimum and curvature strongly dependent on the insulator type and processing parameters, seen in Fig 6. However, the energy at which $\mathrm{N_{SS_{MIN}}}$ was found only varied by ±0.5eV and was determined solely by the semiconductor type. The origin for this continuum of states in the band gap was said to be the bonding disorder in the interface. The model became known as the disorder induced gap states model (DIGS).

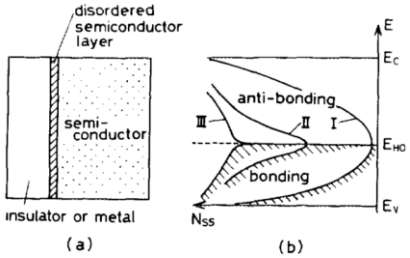

Figure 8. The a) theoretical layer structure at an IS or MS interface and the b) density of states in the gap as a function of energy. DIGS predicts the curvature and magnitude of the U-shaped density of states graph depends on the amount of disorder at the interface. Three levels of disordering are shown I) a good IS interface II) a bad IS interface and III) a typical MS interface [59].

The DIGS model states that the bonding at the either an MS or IS interface will not be ideal and bond lengths along with angles will be perturbed from their ideal orientations. This effect causes a continuum of bonding (donor-like) and antibonding (acceptor-like) states in the gap where the density of states depends on the magnitude of disorder in the interface. Also, the pinning level can be found at the minimum of the U-shaped density of states where the states change from acceptor-like closer to the valence band to donor-like near the conduction band. Pinning occurs due to the fact that coercing the Fermi level at the surface could cause a very large uncompensated charge density at the interface.

Hasegawa and Ohno point out that in most MS interfaces there exists a very thin oxide insulator layer and because the MIGS evanescent tails penetrate 1.5 to 4Å, DIGS becomes the best method of explaining FLP due to its' explanation of disorder in the IS interface. However, it should be noted that at intimate MS interfaces it's likely that the MIGS and DIGS charge neutrality levels are very close and cannot be used to determine the most suitable model [59].

2.3.2.5 Bond Polarization Model

Although it is likely that barrier height variation has a dependence on chemical bonding, very little attention has been given to finding a quantitative solution for bonding induced interface dipoles until a recent paper by Tung. In this paper he shows that by altering the original Schottky-Mott equation with an additional term whose dependence is on the charge density and CNL and relating this density to charge transfer at the MS interface, agreement has been found with experimental data. Assuming only interactions between the closest neighbors in either the semiconductor or metal planes, Tung found an

expression for the charge transfer, Q_M, which he then related to the barrier height of experimental data [60]. The derived equations for total charge transfer and the revised barrier height function are as follows:

$$Q_M = \frac{\phi_M - \chi_S - E_g/2}{E_g + \kappa} \quad \textbf{(9)}$$

$$\Phi_{B,n}^0 = \gamma_B(\phi_M - \chi_S) + (1 - \gamma_B)\frac{E_g}{2} \quad \textbf{(10)}$$

Here, ϕ_M is the metal work function, χ_S, is the semiconductor electron affinity, E_g is the bandgap of the semiconductor and κ is the hopping interaction. The term γ_B has been related to the slope of variation of the barrier height has been found to be

$$\gamma_B = 1 - \frac{q^2 d_{MS} N_B}{\varepsilon_{it}(E_g + \kappa)} \quad \textbf{(11)}$$

where d_{MS} is the bonding length between metal and semiconductor atoms, N_B is the density of bonds at the interface and ε_{it} is the dielectric constant of the interface region estimated as $2\varepsilon_\infty$. Using data from [61], Tung showed that this method was in good agreement with experimental data.

2.3.3 Image-Force Barrier Lowering

As shown in the previous section, addition of charges at the interface will induce an electric field which in turn causes a perturbation of the barrier height. A similar perturbation of the barrier height is caused by the image-force of the metal surface as seen by carriers near the surface of the semiconductor in intimate MS contacts. The image-force can be described by considering a metal surface in vacuum. As an electron approaches the metal from the semiconductor bulk an electric field perpendicular to the surface is induced. The same field could be modeled with a positive charge equidistant from the surface inside the metal as the electron is from the surface in vacuum. Therefore, the electron begins to feel a larger attractive potential as it approaches the metal surface. The total potential energy is found by integrating this image-force from infinity to its current location and adding an external potential pointing in the direction toward the metal from vacuum. The figure below shows magnitude of fields due to the image-force, an external field and the total potential energy [51].

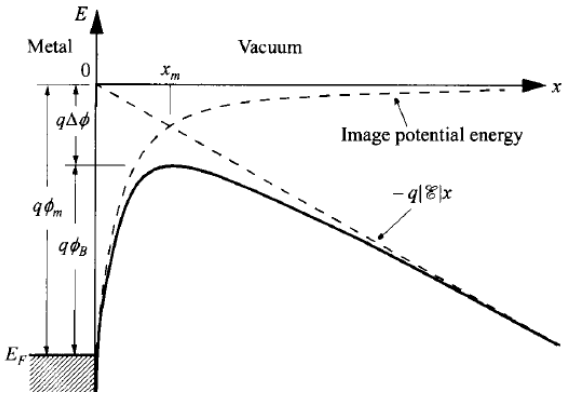

Figure 9. The above diagram shows the vacuum level energy band and the perturbation due to the effect of image-forces and external bias on charges in the vicinity of the metal surface [51].

A similar effect is seen in Schottky barrier heights as seen above in the vacuum level energy band. Because the barrier height and the point where the barrier height is at its peak surface is a function of electric field, or applied bias, measurement methods that assume ideal voltage-independent barrier heights require addition consideration. This will be discussed further in Section 3.2.1.

2.3.4 Homogeneous Barrier Height

Ideally when a metal comes in direct contact with a semiconductor, a laterally homogenous interface is formed and the Fermi level of the metal and semiconductor align. In an n-type semiconductor, electrons close to the junction are unable to screen the electric field generated by the metal surface. Equilibrium is reached when the density of states (DOS) in the semiconductor at the surface shift and atoms near the junction ionize and compensate the electric field. This process is depicted in Figure 6.

In a homogenous Schottky barrier the atoms in the metal and semiconductor are lattice matched and no interface charge exists from defects or impurities. In this case, the Fermi level from the semiconductor lines up with that of the metal and an energy barrier (ϕ_B) is formed with the height:

$$\phi_B = \phi_m - \chi \tag{12}$$

where ϕ_m is the workfunction of the metal and χ is the electron affinity in the bulk semiconductor. Because the bending of the bands is due to a long-range spatially dependent electric field in a material with a non-varying dielectric constant, the variation of charge density is governed by Poissons' equation [53]. Once the boundary conditions are set and the definition of the band bending bias is realized, the solution for the conduction band minimum energy with respect to the Fermi level becomes:

$$\varepsilon_{CBM}(z) = \begin{cases} qV_{bi}\left(1 - \dfrac{z}{W}\right)^2 + qV_N + qV_a, & 0 < z < W \\ qV_N + qV_a, & z > W \end{cases} \tag{13}$$

where W is the depletion region, defined as

$$W = \lambda_D \sqrt{\frac{2qV_{bb}}{k_B T}}, \tag{14}$$

and the Debye length (λ_D) which is given by

$$\lambda_D = \sqrt{\frac{\varepsilon_s k_B T}{q^2 N_D}}. \tag{15}$$

In the above equations V_{bi} represents the built-in voltage, z is the distance into the semiconductor from the MS interface, V_N is the energy difference between the conduction band minimum and the Fermi level in the bulk semicondcutor, V_a is the externally applied bias, and k_B is Boltzmann's constant.

2.3.5 Inhomogeneous Barrier Height

When a metal and semiconductor come into direct contact the likelihood that a perfectly homogeneous interface will occur is very small. Instead, the interface at the MS junction will be made up of many mixed phase patches which results in a barrier height that varies spatially as seen in the figure below. It has also been shown that at an inhomogeneous MS junction, the magnitude of barrier height variation has a strong dependence on not only the size and density of each patch but also the potential

bias, temperature and doping concentration [62, 63]. Because these patches introduce new barrier height dependencies, anomalous measurement results can arise from ideality factors larger than unity, a temperature dependence of the ideality factor, the introduction of the so-called T_0 anomaly, and a reverse-characteristic dependence on bias potential.

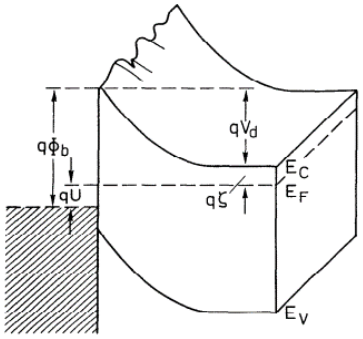

Figure 10. Diagram showing the barrier variation and semiconductor energy band along a 2D plane [64].

2.3.6 Current Transport Mechanism

2.3.6.1 Ideal Thermionic Emission

Bethes' contribution to the development of MS rectifiers was determining thermionic emission (TE) as the correct limiting transport mechanism that governs the current-voltage characteristics of the device. Bethes' theory was based off the assumptions that (1) the barrier height was larger than $k_B T$, the thermal energy, (2) thermal equilibrium is established at the MS junction, and (3) that drift and diffusion currents are negligible so that the quasi-fermi level for electrons remains flat throughout the depletion region. With these assumptions, a quantitative expression for the current magnitude in terms of applied bias can be made. This idealized equation for current density is given below (derivation found in Appendix A).

$$J(V_A) = A^* T^2 \exp\left(\frac{-q\phi_b}{kT}\right)\left[\exp\left(\frac{qV_A}{k_B T}\right) - 1\right] \quad \textbf{(16)}$$

Where,

$$A^* = \frac{4\pi m^* q k^2}{h^3} \quad \textbf{(17)}$$

also known as the Richardson constant.

One assumption made in the derivation of the above thermionic emission rate limited current-voltage relationship is that the applied voltage bias is dropped across the MS junction. In reality voltage is dropped over various series components such as the metal contacts to the semiconductor material and the junction between the two. Assuming this resistance is independent of the applied voltage, Equation (16) must be altered to show the true voltage drop across the junction. The magnitude of series resistance in a device can be easily found graphically, this process is described in Section 3.1.2.

$$J(V_A) = A^* T^2 \exp\left(\frac{-q\phi_b}{k_B T}\right)\left[\exp\left(\frac{q(V_A - qI_{SB}(V_a)R_s}{k_B T}\right) - 1\right] \quad \textbf{(18)}$$

Although the above equations are suitable for describing thermionic transmission over an ideal voltage-independent barrier, further consideration needs to be taken to account for non-deal properties

of the MS junction. The potential stemming from image forces shifts the peak barrier height inside the semiconductor along with establishing a slight barrier height dependence on the applied voltage. A revised equation is given below. Notice in the equations below that the saturation current density (J_0) now includes a term that describes the barrier height offset ($\Delta\phi_{bi}$). The ideality factor, η, can be described as a catch-all for the barriers dependence on voltage originating from known and/or unknown sources. A more detailed treatment of the non-ideal current density versus voltage (J-V) relationship can be found in Appendix B.

$$J_0 = A^* T^2 \exp\left(\frac{-q(\phi_{b0} - \Delta\phi_{bi})}{k_B T}\right) \quad \textbf{(19)}$$

$$J(V_A) = J_0 \exp\left(\frac{qV_A}{\eta kT}\right)\left[1 - \exp\left(\frac{-qV_A}{k_B T}\right)\right] \quad \textbf{(20)}$$

2.3.6.2 Thermionic Field Emission and Field Emission

Thermal emission over the barrier is likely the most prominent current transport mechanism in lightly doped MS junctions; however in highly doped semiconductors the smaller barrier thicknesses increase the probability of quantum tunneling. Since the lateral thickness of the barrier decreases at elevated energy levels, the tunneling probability increases, however, the density of thermally activated carriers decreases. This results in a distribution of transmitted carriers at an energy level lower than the peak barrier height which effectively manifests itself as an additional lowering of the barrier height. Current contribution from this process is known as thermionic field emission (TFE). In the case of heavily doped semiconductors where the Fermi level resides above the conduction band minimum, barrier thickness at energies near the Fermi level can allow significant tunneling. This process is known as field emission (FE) [52]. The current contribution from tunneling can be expressed as:

$$I_{TFE} = I_{S-TFE}\left[\exp\left(\frac{qV_a}{E_0}\right) - 1\right] \quad \textbf{(21)}$$

Where I_{S-TFE} is the saturation current for TFE and the energy E_0 is given as,

$$E_0 = E_{00} \coth\left(\frac{E_{00}}{k_B T}\right) = \frac{\eta k_B T}{q} \quad \textbf{(22)}$$

The ideality factor η represents deviations from ideal TFE and the energy E_{00} is a characteristic of the bulk semiconductor and is given as,

$$E_{00} = \frac{e\hbar}{2}\sqrt{\left(\frac{n}{\varepsilon_s m^*}\right)} \quad \textbf{(23)}$$

where n represents the effective carrier concentration in the semiconductor, m^* is the electron mass in the semiconductor and ε_s is the static permittivity of the semiconductor.

It can be seen from the above equations that the domination of a particular current transport method is dictated primarily by the doping density. According to Schroder [65], TE is considered the dominate current transport process when $E_{00} \leq 0.5kT$, TFE when $0.5kT < E_{00} < 5kT$ and FE when $E_{00} \geq 5kT$. E_{00} is plotted as a function of doping density for wurtzite GaN and cubic GaAs in Figure 11. For GaN the TE to TFE transition occurs near $7.4 \cdot 10^{16}\ cm^{-3}$ at RT and the TFE to FE transition occurs

near $8.2 \cdot 10^{19}\ cm^{-3}$ at RT. For GaAs the TE to TFE transition occurs near $3.6 \cdot 10^{16}\ cm^{-3}$ at RT and the TFE to FE transition occurs near $4.2 \cdot 10^{19}\ cm^{-3}$ at RT. E_{00} is plotted for GaAs and w-GaN across a wide doping density range in Figure 11.

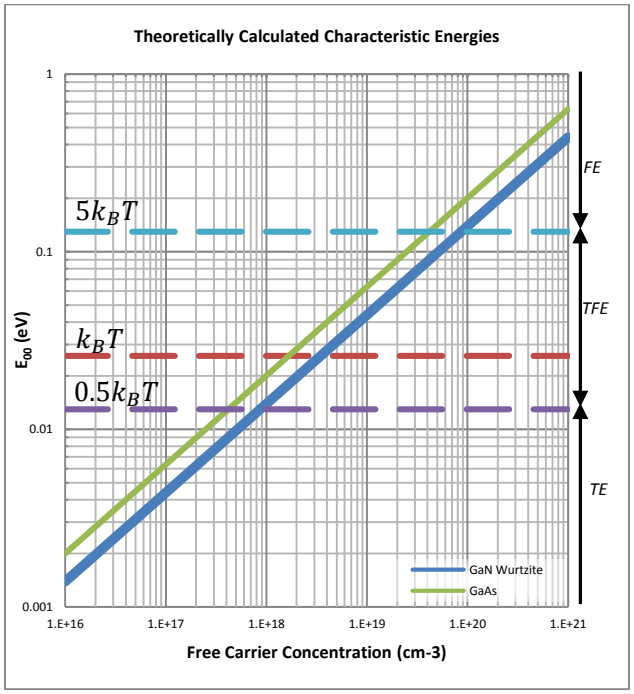

Figure 11. E_{00} ploted as a function of doping density. The dominant current process is shown for a room temperature device with various bulk doping densities.

2.4 Transparent Conducting Oxide Semiconductors

Interest in transparent conducting oxide (TCO) films has been driven by the need for conductive materials which do not block the transmission of light, a characteristic not normally found in materials due to the typical inverse dependence of electronic conductivity and optical transparency in semiconductors. Applications range from electrodes in devices such as photovoltaic's or LED-based displays to providing low emissivity transparent surfaces for energy efficient windows, both of which require conductive contacts to the surface of the device which will not impede the transmission of light either into or out of the material [66, 67]. Indium-tin-oxide (ITO) has been the industry standard in most applications however, due to the rare nature of indium along with the need of TCO's for specialized applications, research has begun focusing on alternatives.

Typical applications of a TCO require more than 80% of visible light transmission and $<10^{-3}\Omega\cdot cm$ to decrease the power loss in a device. This translates to a semiconductor with a larger than $10^{20}\ cm^{-3}$ or higher carrier concentration and a larger than 3eV band gap [68]. Most materials that meet this requirement tend to be n-type due to the high localization of electrons to oxygen atoms around the top of the valence band. Table 3 shows a list of common TCO's and their properties.

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Table 3. List of common TCO's and their properties.

Material	Resistivity ($\Omega \cdot$ cm)	Transparency (%)	Type	Deposition	Reference
SnO_2	$8 \cdot 10^{-4}$	80	N-type	Sputtering	[69]
$In_2O_3{:}Sn\ (ITO)$	$2 \cdot 10^{-4}$	> 80	N-type		
$In_2O_3{:}Ga\ (IGO)$	$2 \cdot 10^{-4}$	85	N-type		
$In_2O_3{:}F$	$2 - 5 \cdot 10^{-4}$	85	N-type		
$Cd_2SnO_4\ (CTO)$	$2 \cdot 10^{-4}$	85	N-type		
$Zn_2SnO_4(ZTO)$	$1 \cdot 10^{-4}$	90	N-type		
$ZnO{:}In$	$8 \cdot 10^{-4}$	85	N-type	Spray Pyrolysis	[70]
$CuAlO_2$	1	75	P-type		[71]
RuO	$4 \cdot 10^{-5}$	-	-	Sputtering	[72]

2.4.1 Ruthenium Dioxide

It was found when Ruthenium is heated in an oxygen environment RuO_2 is formed and is normally deposited by reactively sputtering ruthenium in an oxygen ambient however electrodeposition, chemical vapor deposition (CVD) and thermal evaporation with annealing have also been shown to work. The film normally crystallizes in a rutile-type structure but has been shown to form into a $CaCl_2$ structure or pyrite structure under pressure and has been observed to preferentially oxidize as RuO_2. Its structure leads to a larger than 5eV work function and ~40μΩ·cm film resistivity [72-74].

Ruthenium dioxide was first studied as an oxygen/chlorine evolution anode then its usefulness in electronic circuits became apparent. When oxidized, the film becomes more transparent at visible wavelengths and electrically conductive making it useful for contacts to optoelectronic structures such as photodetectors. In these applications it's necessary to make ohmic or Schottky contacts to the material without impeding photons entering or exiting the material thereby lowering device efficiency. In addition to its optical and electrical properties, RuO_2 has also been shown to be thermally stable making it suitable as a diffusion barrier in electronics requiring thermal stability at high temperatures [72].

3 Methods of Parameter Extraction

3.1 Homogenous MS Junction

As Bethe proposed, in Schottky devices the current limiting process is thermionic emission over the barrier from carriers entering the semiconductor from the metal and vice-versa as given by Equation (16). If deviation from theory occurs a more rigorous model is required to successfully explain experimental data. Assuming thermionic emission over a single barrier, Schottky devices can be characterized using the I-V, C-V and I-V-T methods detailed below.

3.1.1 Thermionic Emission Parameter Extraction

Simply considering Equation (16), a cleverly plotted graph can be used to determine the saturation current (I_S), barrier height (ϕ_B^{IV}), and ideality factor (η). First, assuming the series resistance is negligible, the saturation current is found by plotting the I-V data on a semilog-y plot and extrapolating the y-axis intercept from a linear fit to data gathered at voltages greater than the thermal voltage. Because the plot does not start to show a linear trend until voltage values greater than the thermal voltage, a more useful method is to plot the quantity $I/\left(\exp\left(\frac{qV_a}{kT}\right) - 1\right)$ on a semilog plot thus making the full range of data

linear [65]. Each of these methods is shown in Figure 12. Also, note that examining the slope of the fitted data produces a simple method for extracting the ideality factor (η) in the form of Equation (24).

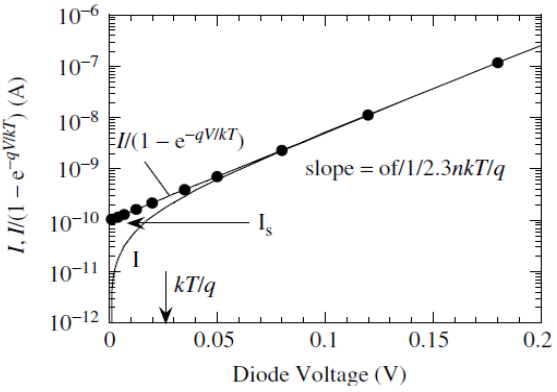

Figure 12. Two graphical methods used to extract the saturation current and ideality factor from IV data collected from an ideal Schottky device [65].

$$\eta = \frac{q}{k_B T}\left[\frac{\partial \ln(I)}{\partial V_a}\right]^{-1} \quad \textbf{(24)}$$

Finally, using the value found for saturation current, the barrier height can be extracted. Rearranging the saturation current equation, the barrier height (ϕ_B^{IV}) takes the form of Equation (25).

$$\phi_B^{IV} = \frac{k_B T}{q}\ln\left(\frac{AA^* T^2}{I_S}\right) \quad \textbf{(25)}$$

Here the barrier height extracted from the current-voltage characteristic depends on the Boltzmann's constant k_B, temperature T, area of the schottky contact A, theoretical Richardson constant A^*, and the saturation current I_S.

3.1.2 Series Resistance Parameter Extraction

Although these methods serve to quickly extract data, they fail to accurately express real world Schottky barriers which tend to suffer from series resistance and a voltage dependent barrier height. Werner [75] pointed out that both series and shunt resistance can dominate the I-V characteristics of a diode leaving only a small regime usable for extracting data. Utilizing the small signal conductance, Werner shows three graphical methods to extract the ideality factor and series resistance (R_s). The results can then be used to modify the I-V data so that correct results for the saturation current and barrier height can be extrapolated. Although there are other methods based on the small signal conductance, Werners method does not require AC signals [76, 77] or artificial functions [78, 79].

If the thermionic emission equation is modified to account for the voltage drop across a series resistance, the effective conductance can be defined as $G = \partial I_d/\partial V$. Dividing the effective conductance by the diode current and plotting the result, Werner shows that a linear trend emerges allowing series resistance and ideality factor to be extrapolated from the horizontal-axis and vertical-axis intercepts respectively. Additionally, this equation can be manipulated for use in two other plots which produce linear trends with an easily extractable ideality factor and series resistance. The identities and resulting equations are shown in the table below.

Table 4. Three equations used to extract the ideality factor and series resistance from a single I-V curve [75].

	Method 1.	Method 2.	Method 3.
Identity	$G = \frac{\partial I_d}{\partial V}$	$\frac{1}{G} = R_{dr}$	$R_{dr} = \frac{1}{G} = \frac{\partial V}{\partial I_d} = \left(\frac{1}{I_d}\right)\frac{\partial V}{\partial\, lnI_d}$
Equation	$\frac{G}{I_d} = \frac{\beta}{n}(1 - GR_s)$	$R_{dr} = \frac{n}{\beta I_d} + \frac{n}{\beta}$	$\frac{\partial V}{\partial\, lnI_d} = R_s I_d + \frac{n}{\beta}$

Assuming the parallel resistance is much larger than the series resistance, the parallel resistance can be extrapolated by examining the reverse bias conductance ($G_{reverse}$) and noting that:

$$G_{reverse} = G_p = \frac{1}{R_p} \tag{26}$$

3.1.3 Capacitance-Voltage Parameter Extraction

Like the current-voltage measurement method, capacitance-voltage measurements are a popular method capable of accurately characterizing Schottky devices. The capacitance per unit area for an n-type Schottky diode is given by

$$\frac{C}{A} = \sqrt{\frac{q\varepsilon_r\varepsilon_0(N_D - N_A)}{2\left(V_{bi} + V - \frac{k_B T}{q}\right)}} \tag{27}$$

where V_{bi} is the build-in potential at the edge of the depletion region. The barrier height is the addition of this built-in potential and the energy difference between the conduction band minimum and the Fermi level (V_0), where $V_0 = k_B T/q\, \ln(N_c/n)$ assuming that $n = (N_D - N_A)$ and all dopants are ionized. Plotting the quantity A^2/C^2 versus the applied reverse bias, V, the slope and the V-axis intercept (V_{int}) can be utilized to extract the effective free electron density and barrier height respectively [65].

$$N_D - N_A = \frac{2}{q\varepsilon_r\varepsilon_0}\left[\frac{\partial\left(\frac{1}{(C/A)^2}\right)}{\partial V}\right]^{-1} \tag{28}$$

$$\phi_B = -V_{int} + V_0 + kT/q \tag{29}$$

It should be noted that even in inhomogeneous junctions, the barrier height extracted from C-V measurements is identical to a homogenous junction whose barrier is the average of the laterally inhomogeneous junction. This comes about because the total space charge at the junction is controlled solely by the average barrier height and free carrier concentration near the interface [53].

3.1.4 I-V-T Analysis of Homogeneous MS Junctions

In principle the Richardson constant for a semiconductor can be derived from the properties of the bulk semiconductor. However, there is large scatter among the values reported in the literature (See Appendix B.) most of which are far from the ideal value calculated from the bulk semiconductor electron

mass. Thus it has become common practice to construct Richardson plots from I-V data to extract the Richardson constant.

From Equation (16) for values of voltage much larger than $k_B T$ the second exponential decays to zero and can be rewritten as:

$$\ln\left(\frac{I}{T^2}\right) = \ln(AA^*) - q\left(\phi_B - \frac{V}{\eta}\right)/k_B T \qquad \textbf{(30)}$$

Thus a Richardson plot can be created by plotting $\ln(I/T^2)$ versus $1/T$ for a voltage larger than $k_B T$. The value of the vertical-axis intercept is related to the Richardson constant by $\ln(AA^*)$. Additionally, for an ideality factor determined by other means, the barrier height can be extracted from the slope. If the ideality factor is unknown the saturation current (I_s) can be used in place of I so that $V \to 0$ and the ideality factor term is cancelled [65].

3.2 Inhomogeneous MS Junction

As mentioned in Section 2.3.5, a metal-semiconductor junction rarely forms with a barrier height that does not vary spatially within the interface plane. Assuming the spatial variation of the barrier height is small compared to the thickness of the charge neutral region, a good approximation can be made by modeling total current as the summation of current through each patch i.e. parallel diodes with different characteristics. However, if barrier height is wildly varying spatially, electric potential saddle points can form inside the semiconductor thereby requiring an even more detailed analysis.

Sullivan et al. [62] numerically simulated MS junctions with patches of inhomogeneity showing the effects of patch size, patch geometry, barrier pinning level, semiconductor doping density, applied bias, temperature, and others. It was shown that barrier height inhomogeneity, when not accounted for, can manifest itself as phenomena interpreted as thermionic field emission or as non-ideal behaviors such as discrepancy in I-V versus C-V extracted barrier heights and ideality factors larger than 1. Thus experimental I-V data alone cannot be used to definitively identify the dominant current transport mechanism in Schottky devices with ideality factors larger than unity.

3.2.1 I-V-T Analysis of Inhomogeneous MS Junctions

The above approach to finding the Richardson constant assumes that a homogeneous barrier exists laterally across the whole area of the diode. Werner et al. has shown that a better approximation of the Richardson constant can be approached if the barrier height and ideality factors are expressed as a function of temperature and used to investigate the properties of a Gaussian distributed lateral barrier height inhomogeneity at the MS interface [64]. Additionally, this approach gives physical meaning to the ideality factor, normally used as an indicator of device quality, defining it as the voltage dependence of the Gaussian mean and standard deviation. Assuming that the distribution of barrier heights in fact can be described by a Gaussian distribution, the probability of finding a particular barrier height ($P(\phi_b)$) can be described as,

$$P(\phi_b) = \frac{1}{\sigma_s\sqrt{2\pi}} e^{\frac{-(\bar{\phi}_{b0}-\phi_b)^2}{2\sigma_s^2}} \quad (31)$$

and

$$\phi_b = \bar{\phi}_{b0} - \frac{q\sigma_{s0}^2}{2k_BT} \quad (32)$$

$$\frac{1}{\eta} - 1 = \rho_2 - \frac{q\rho_3}{2kT} \quad (33)$$

In the equations above, $\bar{\phi}_{b0}$ describes the mean zero-bias barrier height and σ_{s0} describes the zero-bias standard deviation. Plotting the extracted barrier height (ϕ_b) and ideality factor (η) versus a wide range of $q/2k_BT$ should yield a graph with linear portions each of which correspond to a patch with different Gaussian distribution characteristics. Here the variables ρ_2 and ρ_3 represent the dependence of the mean barrier height and standard deviation on applied bias respectively and follow the equations below.

$$\Delta\bar{\phi}_{b0} = \rho_2 \cdot V \quad (34)$$

$$\Delta\sigma_{s0}^2 = \rho_3 \cdot V \quad (35)$$

The equation for saturation current density limited by thermionic emission over a barrier height can then be rewritten to include a temperature and bias dependent barrier height.

$$J_0 = A^*T^2 e^{\frac{q\left(\bar{\phi}_{b0}+\rho_2\cdot V-\frac{q\sigma_{s0}^2+\rho_3\cdot V}{2kT}\right)}{k_BT}} \quad (36)$$

The Richardson plot can then be modified simply by substituting Equation (32) into (30) and re-plotting for each range of temperatures relating to a different patch.

$$\ln\left(\frac{I_S}{T^2}\right) - \frac{q^2\sigma_{s0}^2}{2k^2T^2} = \ln(AA^{**}) - \frac{q\bar{\phi}_{ap}}{kT} \quad (37)$$

As will be shown later, this method produces Richardson constants close to the predicted value for gallium arsenide and gallium nitride.

3.2.2 Reverse Current-Voltage-Temperature Measurements

It has also been shown [80, 81] that a relation between reverse current and temperature can be used to shed light on reverse current conduction mechanisms. Although assumed to be constant by the thermionic emission Schottky equation, the non-ideal reverse current can be perturbed by tunneling, thought to be one of the sources of wildly varying Richardson constants in the literature. According to the following equations, the examination of reverse current can yield yet another method of determining the doping, Richardson constant and effective barrier height.

$$J_{ms} = \frac{A^*T}{k_b}\int_0^{qV_b} F_m T(\eta)(1-F_s)d\eta \quad (38)$$

$$T(\eta) = \exp\left(-\frac{\eta^{3/2}}{E_{00}\sqrt{qV_b}}\right) \quad (39)$$

$$E_{00} = \left(\frac{8}{3}\sqrt{\frac{m^*\varepsilon_s}{n}}\frac{1}{q\hbar}\right)^{-1} \quad (40)$$

Here the current density is limited by the number of carriers able to tunneling from the metal to the semiconductor through the barrier. Equation (38) shows that this can be expressed by summing up the number of carriers at and above the conduction band minimum energy. F_m is the Fermi function of the metal, F_S is the Fermi function in the semiconductor normally approximated as zero, and $T(\eta)$ represents the tunneling probability at some energy (η) below the barrier down to the metal Fermi level. The quantity V_b represents the band built-in voltage caused by the MS junction. The characteristic energy (E_{00}) figure describes the transparency of the barrier and depends on the electron mass (m^*), dielectric constant (ε_s), and effective carrier concentration (n).

3.3 Measurement Acquisition

Each diode was characterized with the current-voltage-temperature (I-V-T), and the capacitance-voltage (C-V) methods. I-V characterization was executed using the Keithley 2400 source meter and temperature control was accomplished in an MMR variable temperature micro probe system under vacuum (<5 mTorr) between 170K and 330K. Capacitive measurements were taken with an HP4192A impedance analyzer at 300K under the same vacuum conditions. The equipment was connected via a GPIB interface to a computer running a LabVIEW program created by the author. Figure 13 shows the test setup located at Virginia Tech in Holden Hall Rm 307.

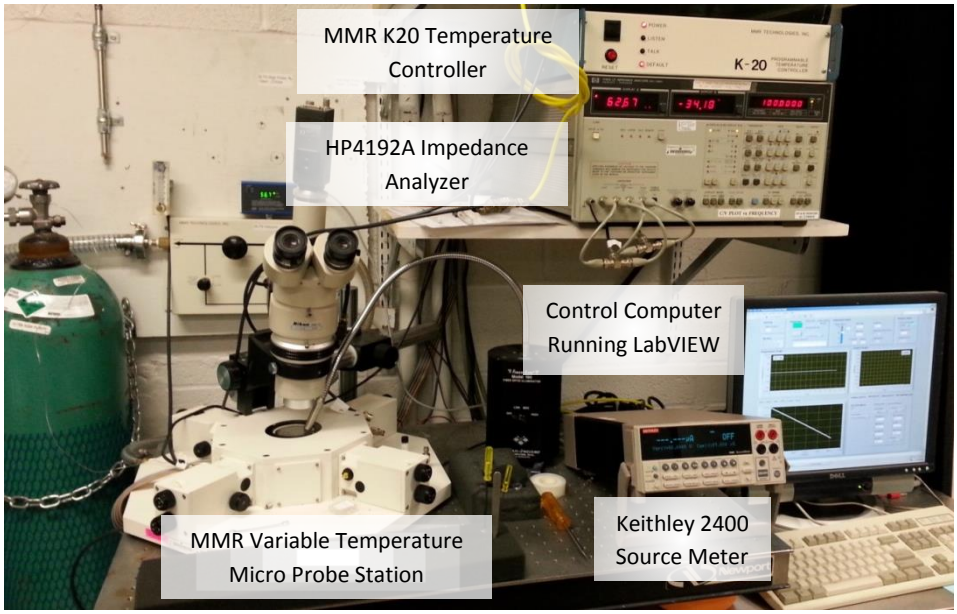

Figure 13. Picture of the measurement setup in Holden 307 capable of J-V-T and C-V-T measurements.

3.4 Device Structures and Fabrication

Fabrication of devices was executed in the Virginia Tech Micro and Nano Fabrication class 10,000 cleanroom. An overview of fabrication can be found below with a more detailed process found in Sections 7.2 and 7.4.

3.4.1 Ni/GaAs Device Structure

Before fabricating the Schottky diodes on GaN with a transparent conducting oxide metal, process qualifications were first carried out on GaAs. GaAs was chosen because it is well characterized in the literature and high quality samples are easier to obtain. The GaAs sample used consists of a 3.92µm device layer on top of a 0.65µm ohmic contact layer grown on a (100) oriented semi-insulating GaAs substrate by MOCVD. The effective carrier concentration by Hall was $2.79 \cdot 10^{16} cm^{-3}$ in the device layer and $5.67 \cdot 10^{17} cm^{-3}$ in the ohmic contact layer. In order to identify processing variabilty, the mask set was designed to yield approximately 144 diodes of six schottky contact areas upon the successful completion of a fabrication run. The diameters of the six schottky diodes range from 200µm to 450µm in steps of 50µm. The a more detailed step-by-step fabrication process can be found in Appendix C.

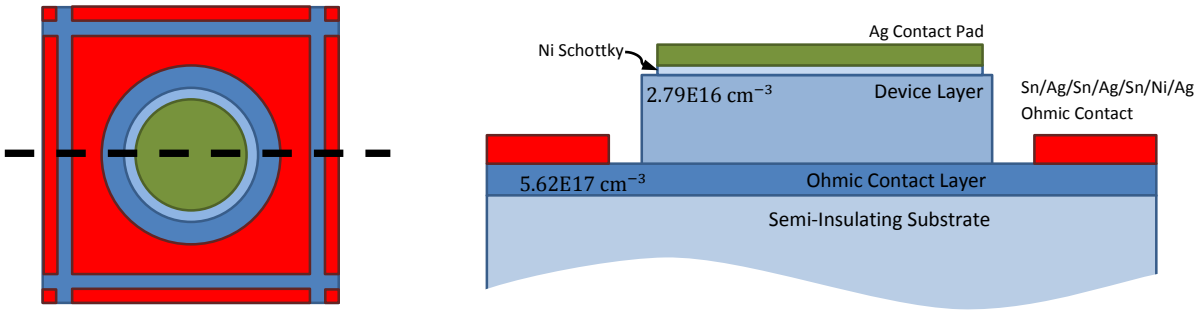

Figure 14. Cross-section of 120530-1 GaAs device structure used for initial Schottky diode fabrication

3.5 Ni/GaAs Schottky Results

Ni/GaAs devices were tested using the evaluation techniques outlined in Section 3.1 and 3.2. This was done to ensure a baseline was set using a well established material prior to applying these methods on a more complex structure. Electrical characterization of the Ni/GaAs sample is shown below and the extracted data is summarized in Table 5.

The forward J-V plot in Figure 16 shows six graphs corresponding to the six different Schottky diode diameters. Current has been normalized to current density by dividing the current at all voltages by the area of the respective Schottky contact. A good indication that current conduction happens across the MS junction and is not hindered by surface conduction is the overlapping of the experimental data over the whole voltage range. The devices show almost no variability with an average barrier height and

standard deviation of 0.889eV and 2.86meV respectively. The average ideality factor and standard deviation is 1.020 and 3.29E-3 respectively. An ideal Richardson constant of 7.56 $A \cdot cm^{-2} \cdot K^{-2}$ was assumed. Series resistance of the devices shown in Figure 16 could not be determined because the data was taken with a compliance level lower than the level at which series resistance becomes dominant.

In the reverse region, the current density was found by first taking the absolute value and then dividing experimental data by the Schottky contact area. This allows the data to be easily plotted on a semilog-y scale. The Ni/GaAs diodes show almost no voltage dependence implying that Thermionic emission is dominant however, two diodes (450um and 350um) display some parallel conduction most likely attributed to either thermionic field emission or thermionic emission over a voltage dependent barrier (image force lowering).

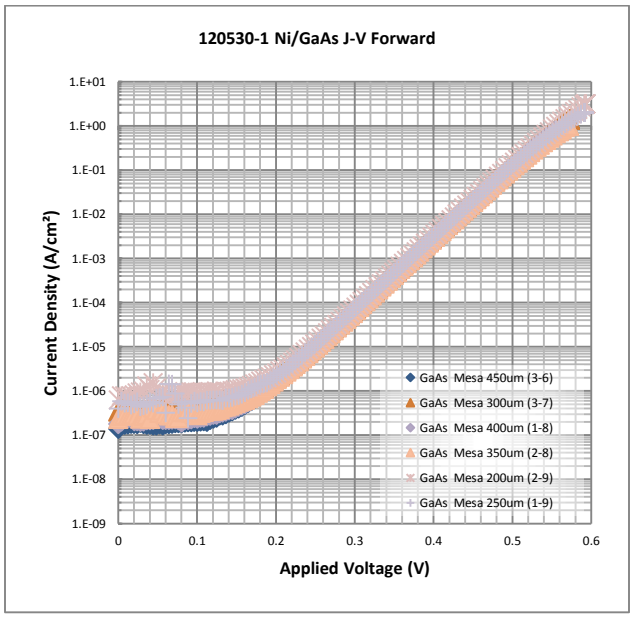

Figure 15. Current density vs. voltage plot of Ni/GaAs Schottky diodes varying in diameter between 200um and 450um.

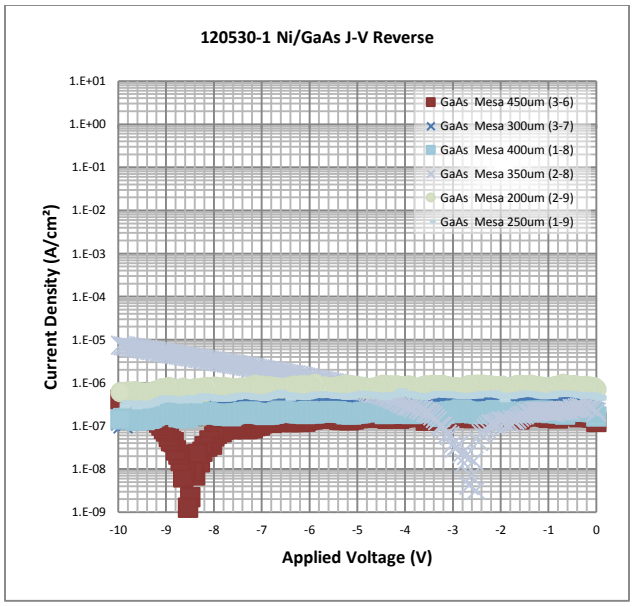

Figure 16. Current density vs. reverse voltage plot of Ni/GaAs Schottky diodes varying in diameter between 200um and 450um.

As described in Section 3.1.3, analysis of experimental data gathered by C-V can yield both a barrier height and the effective carrier concentration profile close to the interface. The capacitance of the 200µm (2-9) Ni/GaAs Schottky diode was measured with an applied bias between 0.2V and -1V (not shown) using a 30mV @ 1MHz AC signal. The quantity A^2/C^2 was then plotted against the applied voltage and a trend line of best fit (using least-squares) was overlaid and extrapolated to the x-axis (Figure 17). According to Equation (28) and Equation (29) the effective carrier concentration and barrier height were extracted using 12.9 for the relative dielectric constant and the density of conduction band states was taken to be $4.7 \cdot 10^{17} cm^{-3}$. It was found that this device had a characteristic barrier height of 0.950eV and an effective carrier concentration of $1.40 \cdot 10^{16} cm^{-3}$, which is in good agreement with the $2.79 \cdot 10^{16} cm^{-3}$ concentration determined from a Hall measurement on a similarly grown single layer film.

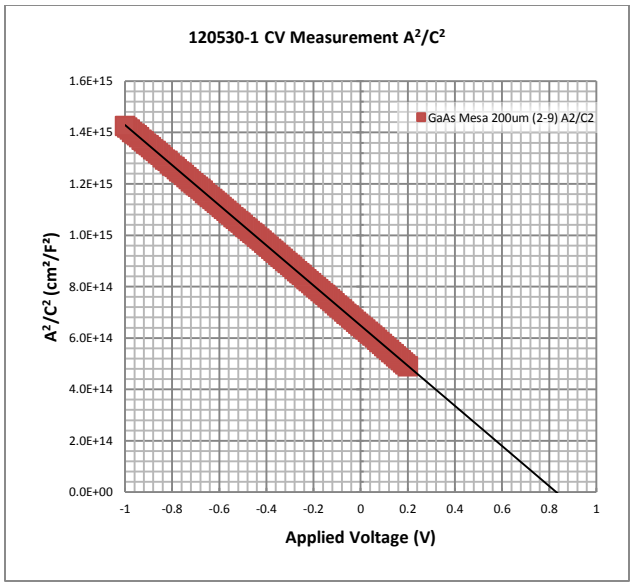

Figure 17. A^2/C^2 plot for the 120530-1 Ni/GaAs Mesa (2-9) devices between 0.2V and -1V. The data was overlaid with a line of best fit using least squares

The effective carrier profile was found by assuming an ideal parallel plate model and relating the capacitance to the depletion width through $W_{dep} = \varepsilon_r \, \varepsilon_0 \, A/C$, where A is taken as the area of the Schottky contact pad and the dielectric constant ε_r as 12.8. The profile can be found in Figure 18. As expected, the profile is flat between the depths of 0.25um and 0.425um from the interface with a concentration of $1.40 \pm 0.097 \cdot 10^{16} cm^{-3}$. To check for consistency, the extracted zero-bias depletion width was compared to the theoretically calculated value using Equations (14) and (15) and the values of 290.79nm and 291.28nm respectively prove the consistency of this approach.

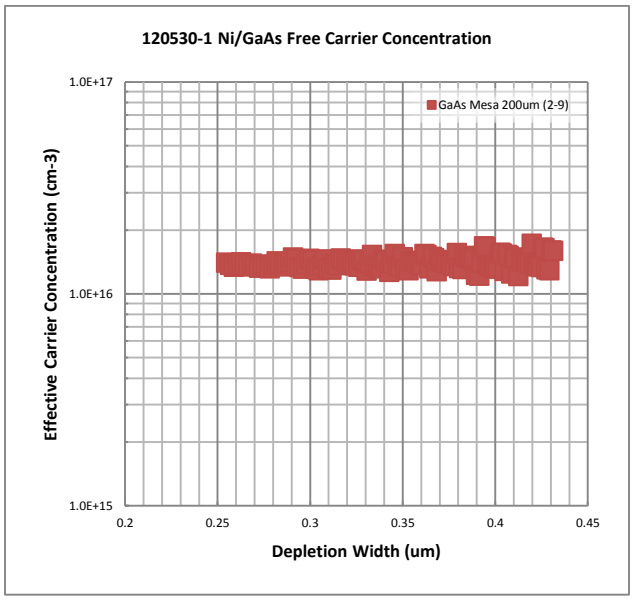

Figure 18. Free carrier concentration profile derived from the slope of the A^2/C^2 data in Figure 18.

Figure 19 shows J-V curves taken under vacuum in an MMR microprobe station between 170K and 330K in steps of 10K. The 'roll-over' at higher voltages can be attributed to series resistance in the film while the saturation at lower voltages and temperatures must be caused by parallel current leakage path but is more likely caused by the test setup. Series resistance determined by Werner's third method at temperatures between 170K and 330K varied between 9.6Ω and 22.7Ω. The temperature dependence of the ideality factor was plotted in Figure 20 according to Equation (22) to extract the characteristic energy and ensure that thermionic emission is the dominant transport method. The experimental data was plotted and fit using the least-squares method yielding a characteristic energy of 1.7meV, a value much smaller than $0.5k_BT$ indicating that thermionic emission should be dominant.

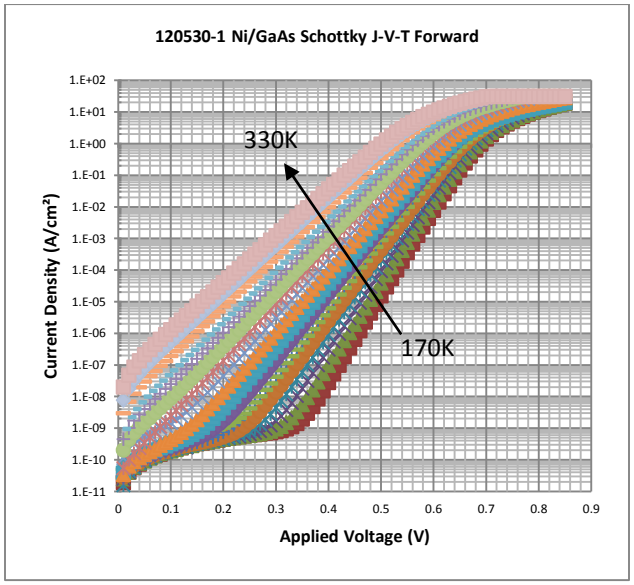

Figure 19. J-V-T plot for the 120530-1 Ni/GaAs sample taken under vacuum between 170K and 330K

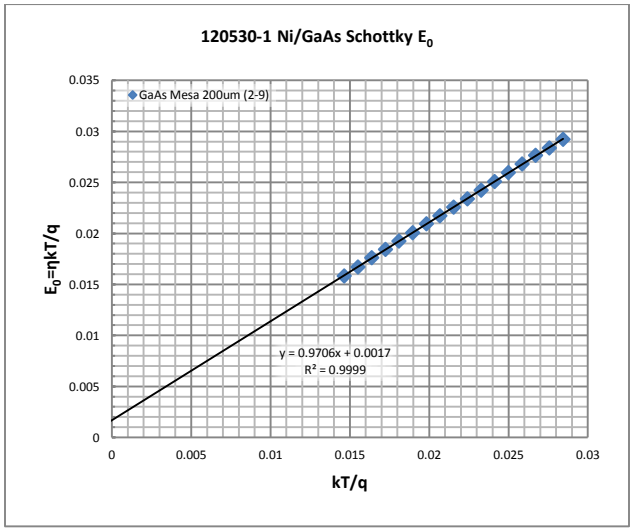

Figure 20. Characteristic energy plot for the 120530-1 Ni/GaAs device plotted between the temperatures of 170K and 330K. The experimental data (scatter) was fitted with a line using least-squares (solid).

Following the details outlined in Section 3.1.4 a Richardson plot was created and the data is shown in Figure 21 with the exception of using the saturation current density instead of current at some voltage. This was done to simplify the equation so that the effect of the ideality factor is cancelled and the area of the diode is already taken into account. The extracted barrier height and Richardson constant are 0.738eV and 0.037Acm^{-2}K^{-2} respectively. Values for the Richardson constant found in the literature are similar to that extracted from Figure 21, however due to the deviation from the theoretical value of 8.04Acm^{-2}K^{-2} indicate that inhomogeneity may exist.

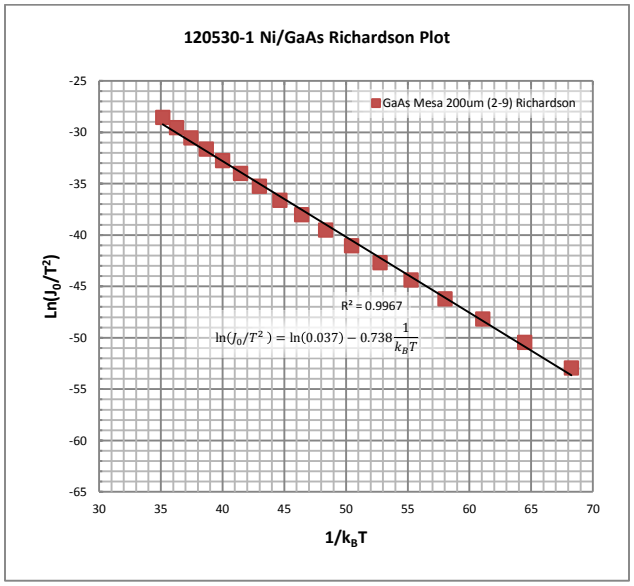

Figure 21. Richardson plot used to extract the effective Richardson constant based on the temperature dependent saturation current density. The experimental data (scatter) is fit with a line (solid line) using least-squares.

As explained in Section 3.2, it is common to have deviation between ϕ_B^{IV} and ϕ_B^{CV} in addition to an extracted Richardson constant that varies greatly from the theoretical value. These inconsistencies have been explained as an inhomogeneity of barrier height laterally at the MS interface. Assuming a Gaussian distribution of barrier heights, Werner et. al. [64] used J-V curves taken at different temperatures to describe the characteristics of the inhomogeneity by quantifying the barrier height and ideality dependence on temperature. This $\phi_B^{IV}(T)$ is used to explain the mean and standard deviation of the barrier distribution while $\eta(T)$ is used to measure the voltage dependence of the two. This method is applied below.

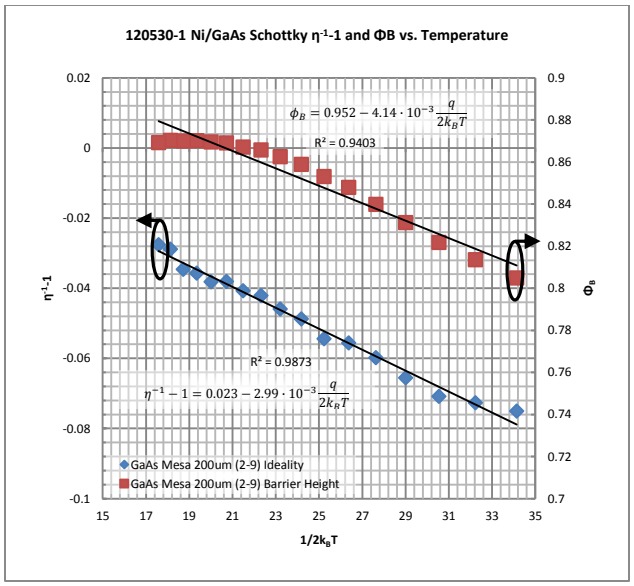

Figure 22. The temperature/bias dependence of the Gaussian distributed barrier heights can be found by fitting the temperature dependence of the barrier height and ideality factor. The experimental data (scatter) is fit with a line (solid line) using least-squares.

Fitting the two lines in Figure 22, it was found that the average barrier height was 0.952eV with a standard deviation of 4.14meV. According to the ideality factor dependence on temperature the mean barrier height has a voltage dependence following $\Delta\phi_B^{IV} = -0.023 \cdot V$ and the standard deviation follows $\Delta\sigma_{s0}^2 = -2.99 \cdot 10^{-3} \cdot V$. To show that the above evaluation of the device fits well with the collected experimental data the theoretical J-V-T curves are calculated using Equation (36) at each temperature and plotted with the original J-V-T calculated as show in Figure 23.

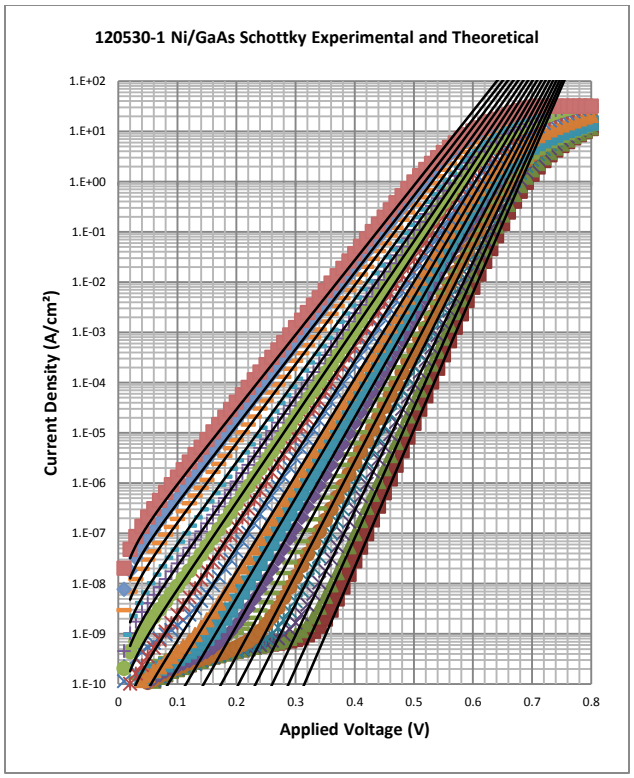

Figure 23. Theoretically calculated J-V-T curves (solid line) between 170K and 330K using Equation (36) and the values extracted from the plot in Figure 22.

Using the standard deviation of the Gaussian distribution the Richardson plot is modified and shown below in Figure 24. The linear fit of the data according to Equation (37) yielded an average barrier height of 0.948eV and a corrected Richardson constant of 6.14Acm^{-2}K^{-2}.

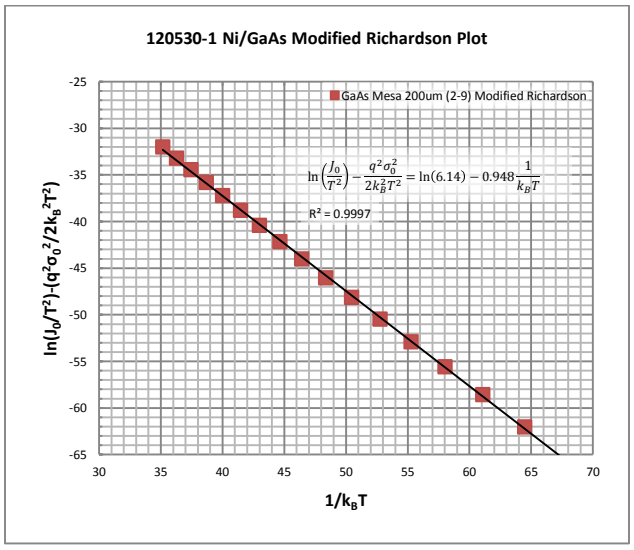

Figure 24. Modified Richardson plot using the standard deviation extracted from analysis of the barrier temperature dependence. The experimental data (scatter) was fit with a line (solid) using least-squares.

Table 5. Summary of extracted data for the Ni/GaAs Schottky diodes

Method	Parameter	Ni/GaAs Schottky 120530-1
I-V	Barrier Height @ 300K (eV) [Std. Deviation]	0.889 [2.86meV]
	Ideality Factor @ 300K [Std. Deviation]	1.020 [3.29E-3]
C-V	Barrier Height @ 300K (eV)	0.950
	Free Carrier Concentration (cm^{-3})	$1.40 \cdot 10^{16}$
I-V-T	Richardson Constant A^{**} (A/K^2cm^2)	0.037
	Richardson Zero-Bias Barrier (eV)	0.738
	Characteristic Energy E_{00} (eV) Experimental : Theoretical	1.7meV : 2.36meV
	Average Barrier Height (eV)	0.952
	Standard Deviation	0.064
	$\rho_2 : \rho_3$	0.023eV : 2.99meV
	Modified Richardson Constant A^{**} (A/K^2cm^2)	6.14
	Modified Richardson Barrier (eV)	0.948

3.6 Discussion of Evaluation Techniques

The I-V, C-V, and I-V-T Schottky evaluation techniques were first employed on Ni/GaAs samples due to the well documented and high quality characteristics of GaAs. It was found that the Ni/GaAs Schottky devices are in fact well behaved with a low series resistance and negligibly small parallel conduction in the forward region. Additionally, the overlapping nature of the current density data for all diodes indicates that the variability from processing is low. In the reverse region, most devices were observed to have a leakage current close to the noise range of the Keithley 2400 with only two of the diodes showing any conduction. The six devices were found to have an average barrier height of 0.889eV with a standard deviation of 2.86meV, a value lower than the theoretical 1.03eV barrier height but not uncommon due to Fermi pinning at the interface. The devices also had an average ideality factor of 1.02 with a standard deviation of 3.29E-3.

Examination of the C-V measurements yielded a larger barrier height of 0.950eV indicating that I-V measurements may be plagued by a non-TE transport mechanisms or that conduction could be dominated by patches of lower barrier height at the interface. In addition to the barrier height, the free carrier concentration was extracted from the slope of the A^2/C^2 plot and found to be n-type with a concentration of $1.40 \pm 0.097 \cdot 10^{16}$. The free carrier concentration was compared to a Hall measurement done on a separate sample consisting of a single layer grown with a recipe similar to the device layer of the 120530-1 sample. Free carrier concentration by Hall measurement was found to be $2.79 \cdot 10^{16}$ and in good agreement with that found by C-V. The doping profile was plotted and found to be in good agreement with the zero-bias capacitance.

In order to study the possible inhomogeneity of barrier heights at the MS interface, I-V-T measurements were taken between 170K and 330K in steps of 10K. The temperature dependent ideality factor extrapolated to yield a characteristic energy of 1.7meV, well below $0.5k_BT$ threshold at room temperature indicating TE is the dominant conduction across the barrier. Next, the saturation current dependence on temperature (Richardson plot) was used to extrapolate a value of $0.037 Acm^{-2}K^{-2}$ which is not in agreement with theory ($8.04 Acm^{-2}K^{-2}$), indicating that inhomogeneity may play a role in current conduction. The barrier height (0.738eV) extracted from the Richardson plot was also low. The

Richardson plot and current conduction equation were corrected upon examination of the barrier height and ideality factor dependence on temperature to find the Gaussian distributed mean barrier height and standard deviation along with the mean and standard deviation dependence on applied bias. Once revised, the Richardson plot yielded a modified Richardson constant of 6.14 $Acm^{-2}K^{-2}$ which is close to the theoretically calculated value and a barrier height of 0.948eV which is in agreement with the mean barrier height, 0.952eV, calculated from the temperature dependence of the zero-bias barrier height. Finally, to check that the values obtained by assuming a Gaussian distribution of barrier heights could successfully describe experimental data, the voltage/temperature dependent barrier height formula was substituted into the Schottky TE equation and the calculations were overlaid on the experimental I-V-T plot. The overlay shows that this method is in good agreement with experimental data.

4 Investigation of RuO_2 Schottky Barriers on GaN

This work focuses on RuO_2/GaN Schottky diodes fabricated by annealing a Ru/GaN diode in open air and the effect on parameters extracted from electrical characterization. To make a comparison, a non-RuO_2/GaN sample was fabricated and tested. Additionally, a Pt/GaN Schottky device was created as a comparison to the current literature. Below is a detailed analysis of the evaluation of these three devices and a summary of the extracted data is shown in Table 6.

4.1 Metal/GaN Device Structure

After processing and characterizing the Ni/GaAs samples the process was adapted for metal/GaN Schottky samples. The GaN devices structure consists of a 1 µm layer on top of a 0.5µm buffer layer. The effective carrier concentration by C-V was $\sim 1E17 cm^{-3}$ in the device layer. These films were grown on a (0001) oriented sapphire substrate by MOCVD. The complete fabrication process is reviewed in Appendix E.

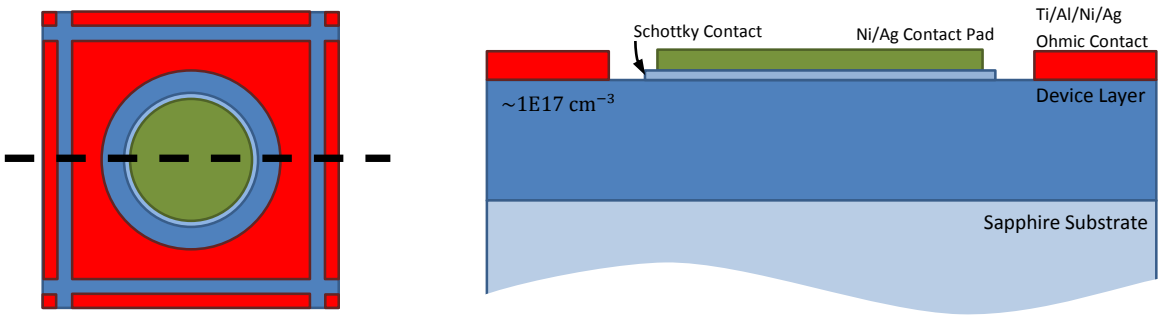

Figure 25. Cross-section of 140128 GaN device structure use for TCO Schottky experiments

4.2 Results of Metal/GaN Schottky Diodes

The forward characteristics of all three diodes are shown in Figure 26. Measurements were taken at room temperature (300K) for multiple devices on each sample but only the 200um devices are shown. As with the GaAs sample, the current was normalized to current density by dividing by the area of the Schottky contact. It was found that the fabricated devices have a larger variation in both barrier height and ideality factor most likely due to the defective nature of GaN. The Pt/GaN Schottky had the largest barrier height of 0.923eV while the annealed and non-annealed Ru/GaN devices had a barrier height of 0.824eV and 0.800eV respectively. An ideal Richardson constant of $24 A cm^{-2} K^{-2}$ was used to extract these parameters. Series resistance calculated by Werner's third method (Section 3.1.2) is 56.85Ω, 57.10Ω, and 55.80Ω for the un-annealed Ru, RuO_2, and Pt Schottky devices respectively.

In the reverse region, the current was normalized using the same method used for the Ni/GaAs. In contrast to the Ni/GaAs sample, these devices in Figure 27 show a voltage dependence conduction mechanism even at low voltages. The low voltage (>-0.75V) current conduction takes the form of Thermionic Field Emission and the conduction at higher voltages (<-0.75V) is still not fully understood. The noise source shown in the reverse characteristics of the Ru sample is currently unknown.

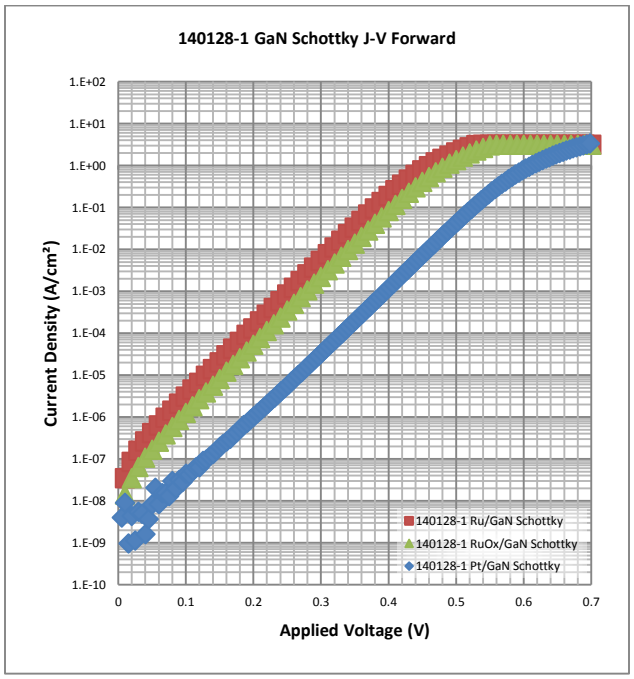

Figure 26. Experimental forward J-V data for the Pt, Ru, and RuO_2 Schottky diodes on GaN

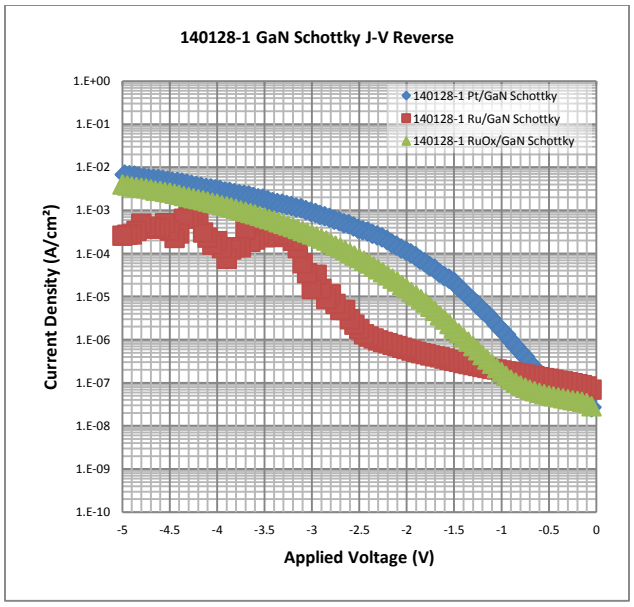

Figure 27. Experimental reverse J-V data for the Pt, Ru, and RuO_2 Schottky diodes on GaN

The GaN Schottky samples were measured between -5V and 0.1V with a 30mV 1MHz AC signal to collect C-V data. Figure 28 shows the A^2/C^2 data gathered for each of the three diodes and overlaid with a line using least-squares. The effective carrier concentration extracted from the slope of the data for the Pt, Ru, and RuO_2 devices is $9.82\pm0.963\cdot10^{16}cm^{-3}$, $9.98\pm0.036\cdot10^{16}cm^{-3}$, and $1.03\pm0.139\cdot10^{17}cm^{-3}$ respectively. The barrier heights computed from the extracted x-axis intercepts are 1.103eV, 0.813eV and 0.857eV for the Pt, Ru, and RuO_2 samples. Extraction of the barrier height was done assuming the relative static dielectric constant of 8.9 and a density of conduction band states of $2.3\cdot10^{14}T^{3/2}$ cm^{-3}. The effective carrier concentration found for Schottky samples fabricated on the 140128-1 GaN material displayed concentration consistent with these values. Additionally, the value determined by Hall on a similarly grown sample was $7.17\cdot10^{16}cm^{-3}$.

By analyzing the change in slope with applied voltage, the effective carrier concentration profile was resolved and plotted in Figure 29. The extracted zero-bias depletion widths for the Pt, Ru, and RuO_2 devices are 94.33nm, 84.29nm, and 85.51nm all of which agree well with theoretical values of 96.99nm, 84.36nm, and 86.00nm.

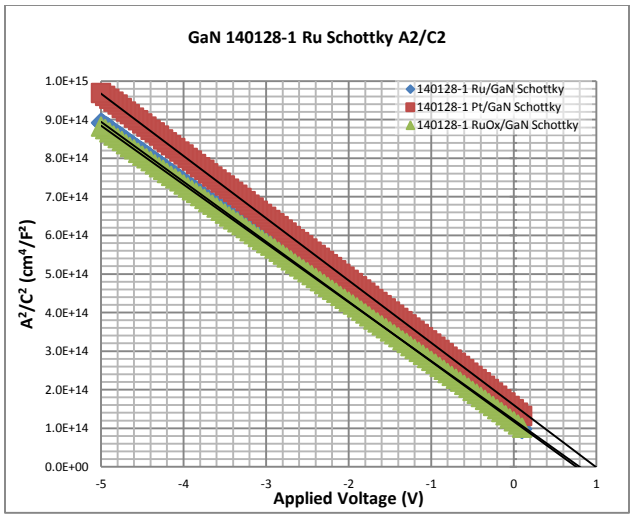

Figure 28. C-V measurements of the Pt, Ru, and RuO_2 Schottky dioes. A line of least-squares fit (solid line) is overlaid on the experimental data (scatter).

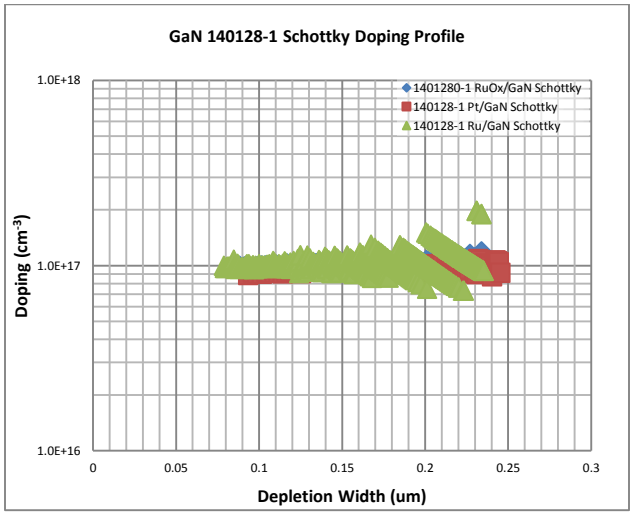

Figure 29. Doping profile for the Pt, Ru, and RuO_2 Schottky samples on GaN

Figure 30 shows J-V curves taken between 170K and 330K in steps of 10K under vacuum for the three diodes. The series resistance was extracted for each diode for each temperature using Werner's third method. The Pt/GaN devices had an average series resistance of 45.9±3.9Ω, the Ru/GaN device has an average series resistance of 58.12±9.79Ω, and the RuO_2/GaN Schottky diode has an average series resistance of 48.10±5.24Ω. The change in resistance with temperature for all three samples showed no strong temperature dependence. Upon examination of each plot, below the series resistance dominated regions, it can be seen that two regions exist. One region at lower voltages, V_A<0.6V for the Pt device and V_A<0.3V for the Ru and RuO_2 devices, has a shallower slope and transitions to a steeper slope at higher voltages, 0.6V>V_A>0.7V for the Pt device and 0.3V>V_A>0.6V for the Ru and RuO_2 devices. This phenomenon will be explained later through a detailed analysis of temperature dependence of the barrier height and ideality factor for each region.

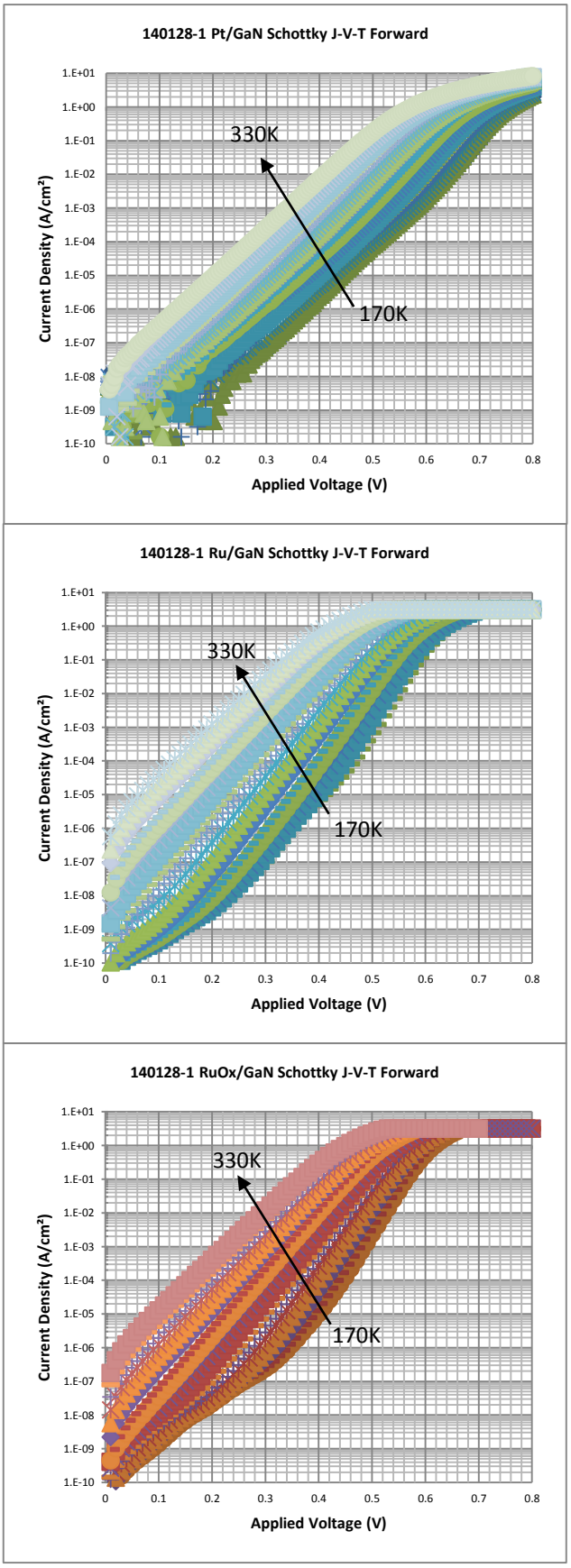

Figure 30. J-V-T experimental data for the Pt (top), Ru (middle), and RuO_2 (bottom) Schottky diodes between 170K and 330K

The characteristic energy is plotted for all three samples in Figure 31. Additionally, each diode was fit in the two voltage regions mentioned above to check the possibility of parallel conduction paths. Each figure has two plots, one of which was created from ideality factors extracted from the lower bias slope and the other from idealities extracted from the region of higher bias. It was found that the values extracted from the higher bias region of the J-V-T plot could be fit with a line using the least-squares method across the whole temperature range while the values extracted from the lower bias regions only showed linearity over a small temperature range. In all three cases the characteristic energy for the higher bias region agrees well with thermionic emission transport according to Figure 11. The extrapolated y-axis intercepts for these devices fall at or below $0.5k_BT$. The smaller range of linearity in the lower bias region is due to two effects. At lower temperature the range of voltage in the lower bias region, which the ideality is extracted from, is dominated by parallel resistance. Secondly, as the temperature is increased, the conduction component associated with the slope at higher bias regions increases more rapidly resulting in the effect in the lower bias region being masked.

Although obvious from the deviation between ϕ_B^{IV} and ϕ_B^{CV}, a Richardson plot (Figure 32) was created to confirm the possibility of inhomogeneity. The experimental data was fit using least-squares over the full range of temperatures. The extracted Richardson constants and barrier heights for the Pt/GaN device is $2.81 \cdot 10^{-7} Acm^{-2}K^{-2}$ and 0.455eV, $0.140 Acm^{-2}K^{-2}$ and 0.672eV for the Ru/GaN device, and $6.27 \cdot 10^{-3} Acm^{-2}K^{-2}$ and 0.599eV for the RuO_2/GaN device respectively. Both the effective Richardson constants and extracted barrier heights are low and stray from theory indicating that thermionic emission over a single barrier height cannot explain these MS junctions.

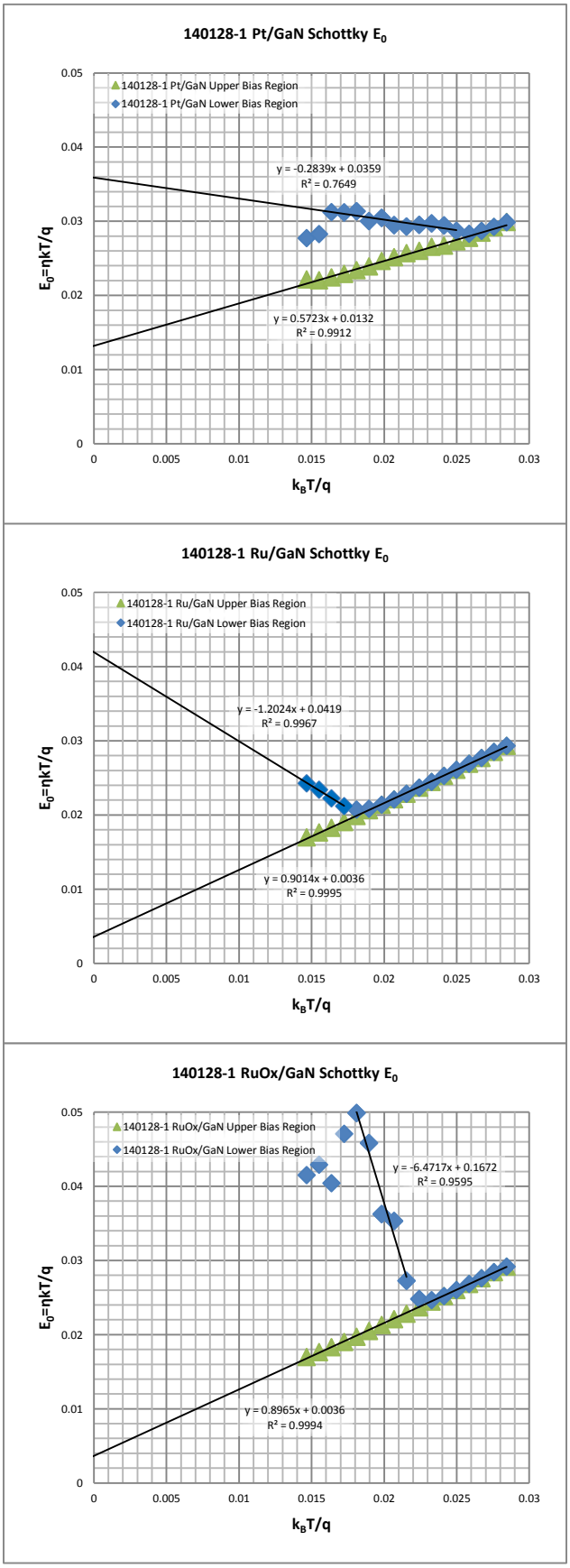

Figure 31. Characteristic Energy plots of the Pt (top), Ru (middle), and RuO_2 (bottom) Schottky devices on GaN. The green scatter represents data extrapolated from the J-V curve at higher biases while the blue curve represents data extrapolated from lower biases. The line of best fit was found using least-squares method over the linear region of each dataset and overlaid on the data.

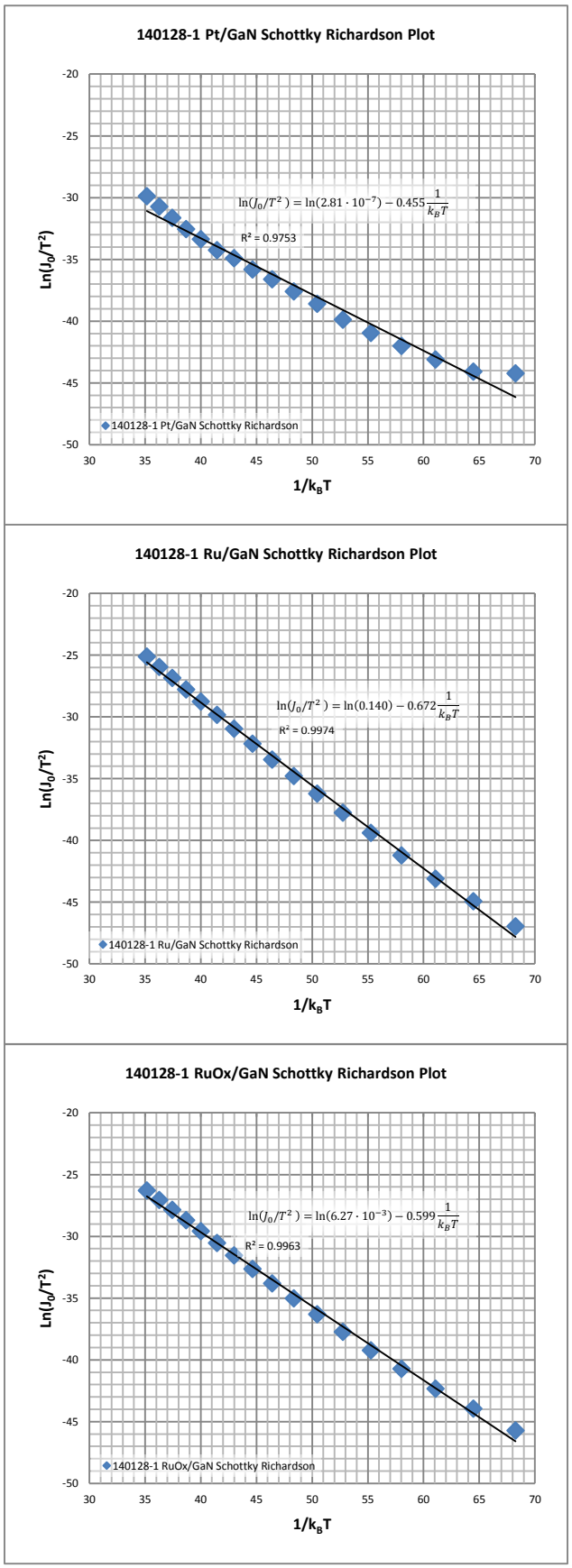

Figure 32. Richardson plots for the Pt (top), Ru (middle), and RuO_2 (bottom) Schottky diodes on GaN. The data (scatter) was fit with a line using least-squares (solid line) and overlaid on the plot.

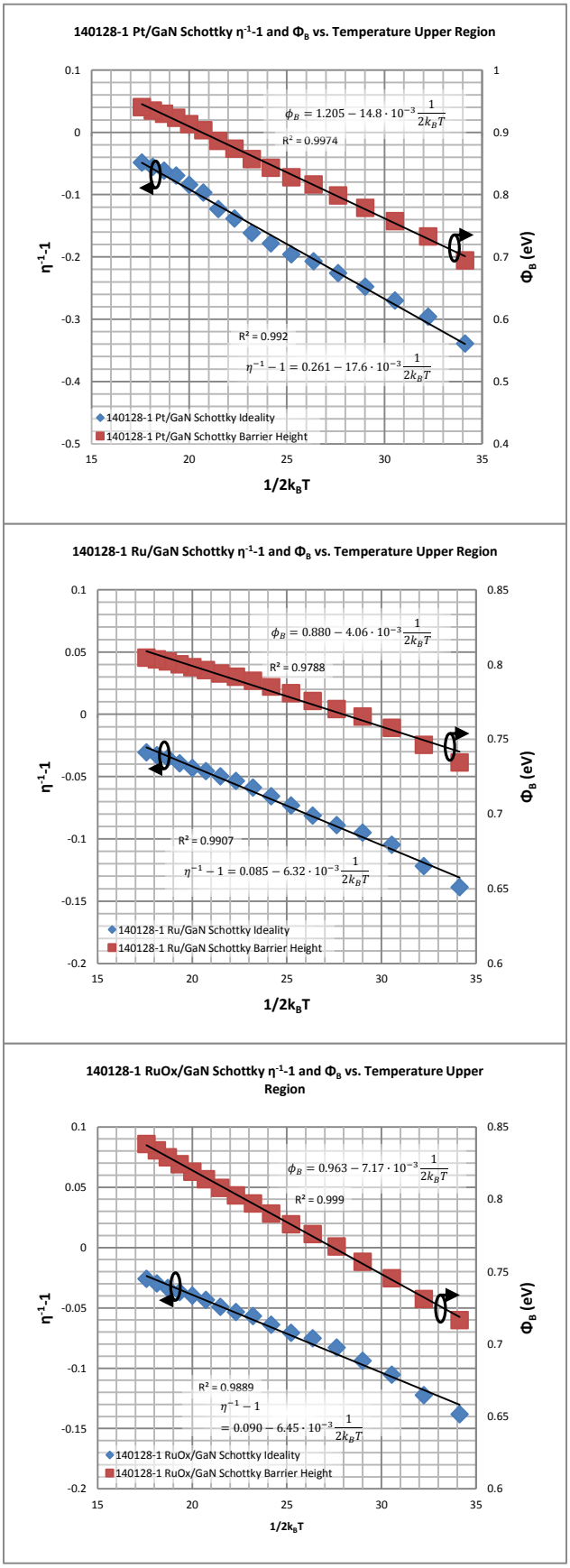

Figure 33. Ideality factor and barrier heights for the Pt (top), Ru (middle) and RuO_2 (bottom) Schottky diodes extracted from higher bias regions ranging in temperature between 170K and 330K. The Pt device is not plotted on the same y-axis scales as the Ru and RuO_2 devices.

The barrier height and ideality factor temperature dependence was plotted for all three devices according to Section 3.2.1 and the experimental data is shown in Figure 33. A line of least-squares fit was overlaid on all plots along with the equation showing the slope and y-axis intercept. The mean barrier height was extracted from the y-intercept while the slope corresponds to the standard deviation of the Gaussian distributed barrier heights. The voltage dependence of the mean barrier height was found from the slope of the η^{-1}-1 temperature dependence while the y-intercept describes the voltage dependence of the Gaussian standard deviation. A summary of the extracted data can be found in Table 6.

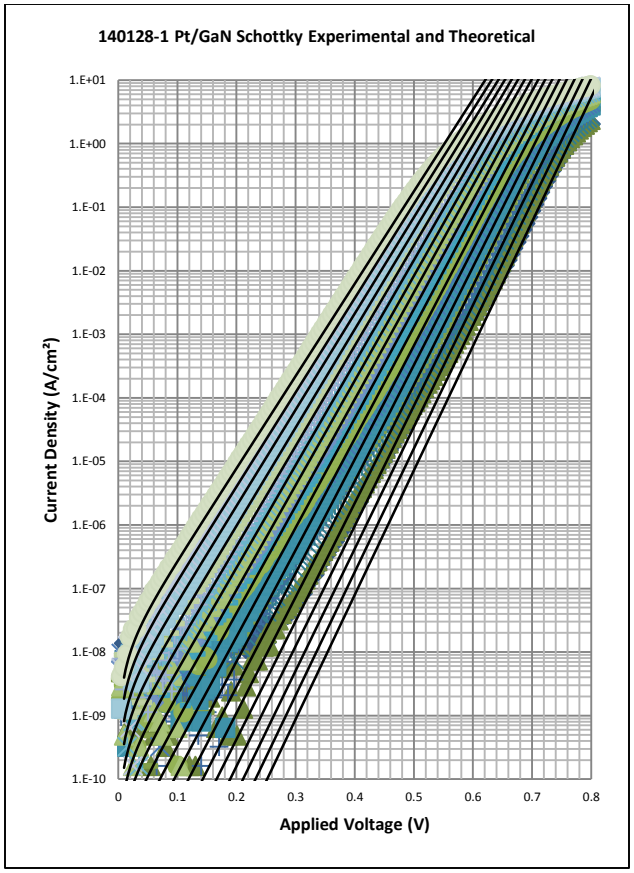

Figure 34. Theoretically calculated J-V-T curves (solid line) for the Pt/GaN device between 170K and 330K using Equation (36) and the values extracted from the plot in Figure 33.

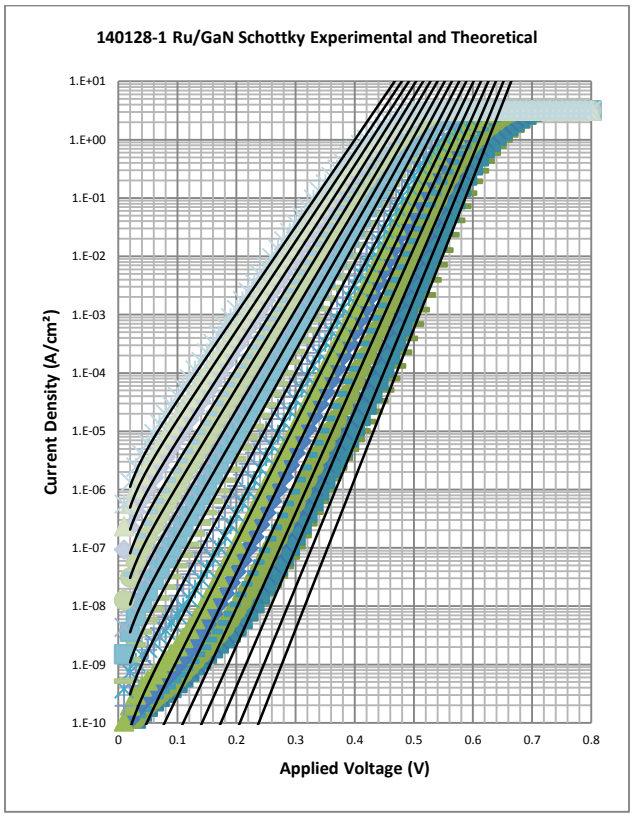

Figure 35.Theoretically calculated J-V-T curves (solid line) for the Ru/GaN device between 170K and 330K using Equation (36) and the values extracted from the plot in Figure 33.

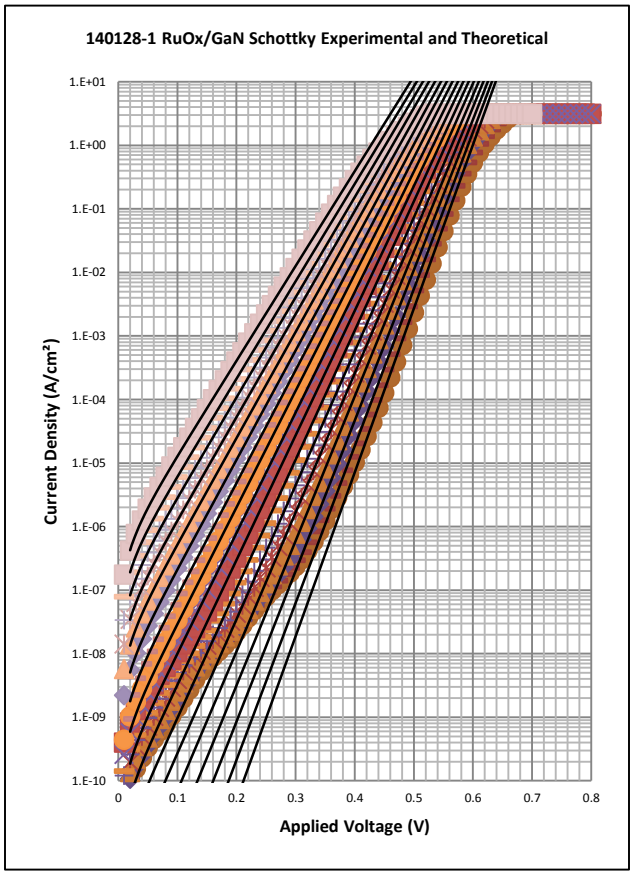

Figure 36. Theoretically calculated J-V-T curves (solid line) for the RuO_2/GaN device between 170K and 330K using Equation (36) and the values extracted from the plot in Figure 33.

To check for consistency, the thermionic emission equation with voltage and temperature dependent saturation current density was calculated for all devices. The agreement of this model with experimental data is made apparent by the overlapping solid lines to with the scatter data at each temperature.

The Richardson plots were corrected using the standard deviations extracted from the barrier temperature dependences and shown below in Figure 37. Fitting the modified Richardson plots with a line using least-squares, the average zero-bias barrier height and modified Richardson constant were extrapolated from the slope and y-intercept respectively. The barrier heights of 1.204eV, 0.878eV, and 0.962eV and modified Richardson constants of 23.69$Acm^{-2}K^{-2}$, 21.09$Acm^{-2}K^{-2}$, and 23.50$Acm^{-2}K^{-2}$ for the Pt, Ru, and RuO_2 devices respectively, agree well with theory and previous calculations.

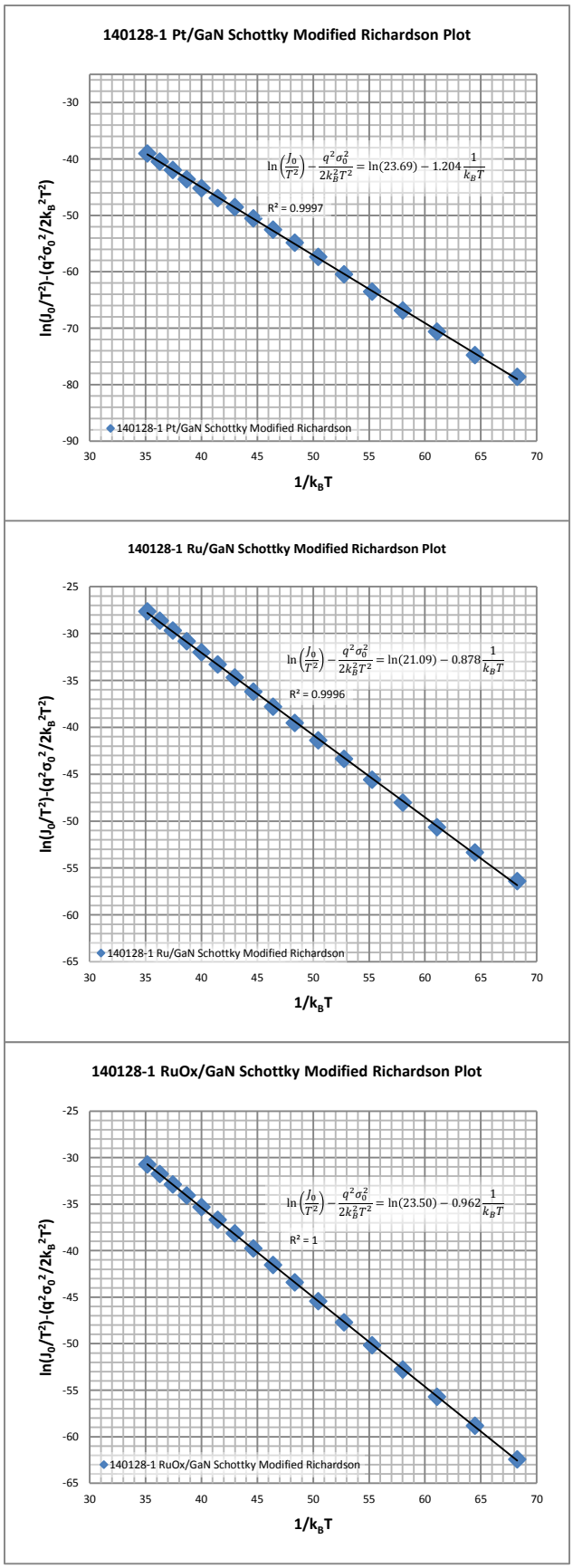

Figure 37. The modified Richardson plots for the Pt (top), Ru (middle) and RuO_2 (bottom) Schottky devices on GaN.

Table 6. Summary of data extracted for devices fabricated on the 140128-1 GaN material

Method	Parameter	Pt	Ru	RuO_2
Theory	Metal Work Function (eV)	5.65	4.71	-
	Theoretical Barrier (eV)	1.55	0.61	-
J-V	Barrier Height @ 300K (eV) [Std. Deviation]	0.954 [20.4meV]	0.785 [11.8meV]	0.809 [-]
	Ideality Factor @ 300K [Std. Deviation]	1.088 [0.036]	1.071 [0.036]	1.031 [-]
C-V	Barrier Height @ 300K (eV)	1.013	0.813	0.857
	Free Carrier Concentration (cm^{-3})	$9.82\pm0.963\cdot10^{16}$	$9.98\pm0.036\cdot10^{16}$	$1.03\pm0.139\cdot10^{17}$
J-V-T	Characteristic Energy (meV)	13.2	3.57	3.63
	Richardson Constant A^{**} (A/K^2cm^2)	0.01	11.01	0.133
	Richardson Zero-Bias Barrier (eV)	0.721	0.793	0.674
	Average Barrier Height (eV)	1.205	0.880	0.963
	Standard Deviation (eV)	$121.7\cdot10^{-3}$	$63.7\cdot10^{-3}$	$85.7\cdot10^{-3}$
	$\rho_2 : \rho_3$	-0.261 : $-17.6\cdot10^{-3}$	$-85.0\cdot10^{-3}$: $-6.32\cdot10^{-3}$	$-90.0\cdot10^{-3}$: $-6.45\cdot10^{-3}$
	Modified Richardson Constant A** (A/K^2cm^2)	23.69	21.09	23.50
	Modified Richardson Barrier (eV)	1.204	0.878	0.962

4.3 Discussion of GaN Device Results

The Pt, Ru, and RuO_2 Schottky devices have been evaluated using the same techniques first employed on the Ni/GaAs sample in Section 3.5. In comparison to GaAs, the presented results show that the Schottky devices fabricated on GaN are more complex in nature. From the testing of multiple devices on the same sample, it was found that the processing variability was larger than that of the Ni/GaAs sample. At larger forward biases, the saturation of the current in the forward region showed almost no temperature dependence indicating that it is most likely caused by series resistance in the bulk GaN or from the ohmic contacts and not non-linear series elements at the MS interface. Review of the literature shows that this check is not commonly done [82-86], bringing into question whether or not the forward characteristics are dominated by temperature dependent circuit elements in a series configuration. Using Werner's third method of resistance extraction, it was found that all three devices had a series resistance around 55Ω again solidifying the idea that it was not caused by a non-ohmic series element. The average barrier heights and ideality factors extracted for each Schottky sample was found to be 0.954eV and 1.088 for Pt, 0.785eV and 1.071 for Ru, and 0.809eV and 1.031 for the RuO_2 devices. The theoretically calculated barrier heights for the Pt and Ru samples are shown in Table 6 and any deviation is considered to be due to Fermi level pinning at the interface.

C-V measurements were taken at room temperature between 0.1V and -5V for a 200um diameter device on all three samples. Linearity of the A^2/C^2 graph indicates that all three samples are doped uniformly throughout the swept depletion widths (80nm to 240nm). The deduced n-type ~$1\cdot10^{17}cm^{-3}$ effective carrier concentration from these three samples was in agreement with samples made with different Schottky metals on the same material in addition to the carrier density determined by Hall ($7.17\cdot10^{16}cm^{-3}$). Upon extraction of the x-axis intercept from the line fit to experimental A^2/C^2 data it was found that the barrier heights from simple J-V measurements where smaller (-59meV for the Pt/GaN device, -28meV for the Ru/GaN device, and -48meV for the RuO_2), a common characteristic seen both in the Ni/GaAs sample and the literature .

The results of the J-V evaluation suggest that by annealing the Ru/GaN device an increase of 24meV in barrier height with a slight decrease in average ideality factor is achieved. By C-V an increase of 44meV was observed. This increase can be attributed to the creation of Ru-O compounds during the annealing process [74].

In a similar study on RuO_2 Schottky contacts deposited by RF magnetron sputtering to GaN, barrier height and ideality factor extracted by J-V were 0.920eV and 1.363 respectively [87]. The larger barrier height can most likely be attributed to the RuO_2 film being more uniformly oxidized compared to our film while the larger ideality factor can be explained by surface damage caused by sputtering the film [88-90]. However, upon examination of the I-V data provided, the diodes reported suffer from a ~10kΩ series resistance at 1V causing the results to be questionable due to pure thermionic emission being assumed. From this same work, the extracted barrier height from C-V measurements was 1.038eV which is larger than the reported value in Table 6 but could be contributed to surface damage. No temperature dependent data was reported. In another study done by Kim et. al. [74] RuO_2/GaN Schottky diodes were fabricated by thermal evaporation of ruthenium followed by annealing in pure oxygen. Only J-V data was reported. It was found that the as-deposited film had a barrier height of 1.29eV with an ideality factor of 1.46 and after annealing at 500°C in pure oxygen, the barrier height increased to 1.43eV and the ideality factor decreased to 1.08.

J-V measurements were performed between 170K and 330K in steps of 10K to study the possibility of inhomogeneity at the MS interface. In all three devices a parallel conduction mechanism dominated much of the J-V curves at lower temperatures for each of the diodes. Extracting the characteristic energy for the higher and lower bias regions of each device made it clear that the parallel conduction mechanism was not thermionic emission however, the linear portion at higher biases was. It was found that the characteristic energies fit to the ideality factors extracted from larger biases fell at or below the $0.5k_BT$ line. Nevertheless, as with the Ni/GaAs devices mentioned previously, the extracted Richardson constant and barrier height fell well below the expected values indicating thermionic emission over a single barrier could not well explain the experimental data.

It was found from Werner's method of fitting the J-V-T results with a Gaussian distributions of barrier heights that Pt has the highest average barrier height of 1.205eV, then the ruthenium dioxide at 0.963eV and the un-annealed ruthenium sample with the smallest at 0.88eV. This pattern is consistent with J-V and C-V measurements. From the ideality factor dependence on temperature it was found that the ruthenium samples shared similar barrier and standard deviation voltage dependencies while the platinum sample suffered from an almost 300% greater dependence for both figures in comparison. This could mean that the platinum sample has smaller areas of large barrier heights which can be perturbed more easily with small changes of voltage whereas the ruthenium samples suffer from a tighter distribution of barrier so that any change will only slightly shift the mean and standard distribution with voltage. The standard deviation figures mentioned previously agree with this synopsis.

The Richardson plot was corrected with the standard deviations and, in all three devices, found to become more linear across the whole temperature range. The zero-bias barrier height extrapolated from the slope was found to be in good agreement with the barrier height temperature dependence data.

Extrapolating the linear portion of the data to the y-intercept the effective Richardson constants found are 23.69$Acm^{-2}K^{-2}$, 21.09$Acm^{-2}K^{-2}$, and 23.50$Acm^{-2}K^{-2}$ for the Pt, Ru, and RuO_2 devices respectively. These values agree well with the theoretically calculated 24$Acm^{-2}K^{-2}$ using an electron mass of 0.2m_0.

Because Werner's method for characterization of inhomogeneity is only suitable for thermionic emission across the barrier distribution, fitting the linear portion of the J-V-T at lower regions wouldn't yield meaningful results. However, displaying the temperature dependence of the barrier height (saturation current) extracted from the lower region yields something interesting. Figure 38, shows both the ideality and barrier height dependence of the lower bias regions on temperature. At larger temperatures (left side of the data), the data is dominated by the thermionic emission barrier heights analyzed above thus drowning out effect from this unknown parallel conduction. At lower temperatures, the extraction of the ideality factor and barrier height become temperature insensitive indicating that parallel resistance (most likely from the test setup) is dominating. Examination of the barrier height data between these two regions yields a straight line corresponding to an average zero-bias barrier height of 1.411eV, 1.375eV, and 1.448eV for the Pt, Ru, and RuO_2 Schottky devices respectively. Additionally, the standard deviation (slope) extracted from these lines is $-26.0 \cdot 10^{-3}$ eV, $-22.4 \cdot 10^{-3}$ eV, and $-29.5 \cdot 10^{-3}$ eV for the Pt, Ru, and RuO_2 samples. This similarity between the three temperature dependence barriers implies that the lower bias region is metal insensitive and may be caused by a material property such as traps at the surface allowing tunneling through the barrier in forward bias. This model is consistent with the fact that it dominates at lower bias and lower temperatures because this is where thermionic emission is the weakest. Additionally, the inverse dependence of the reverse leakage current (Figure 27) on barrier height can be explained by tunneling at a fixed energy below the conduction band minimum. At a fixed energy below the conduction band minimum, as the barrier height increases, the tunneling distance decreases causing leakage current to increase.

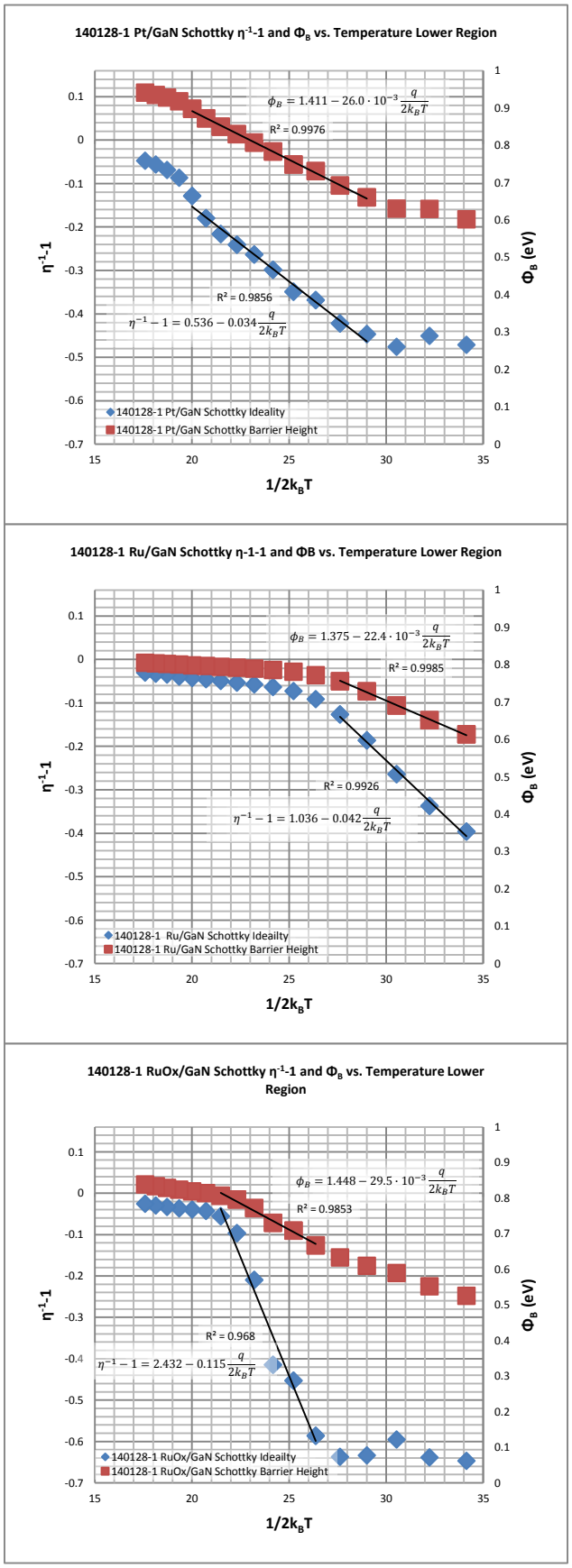

Figure 38. Ideality factor and barrier heights for the Pt (top), Ru (middle) and RuO_2 (bottom) Schottky diodes extracted from lower bias regions ranging in temperature between 170K and 330K.

5 Conclusion

A detailed treatment of Schottky parameter extraction was established and qualified using well behaved Ni/GaAs Schottky diodes. The methods were then applied to investigate RuO_2/GaN devices and compared to the two test cases, Ru and Pt based Schottky devices, fabricated on the same material. Experimental data agreed well with Werner's inhomogeneity approach highlighting the fact that simple I-V parameter extraction usually seen in the literature can result in an incomplete explanation of complicated devices. Ultimately it was found that by annealing ruthenium in open air and 83meV increase in the mean barrier height can be achieved on GaN in addition to the increased film transparency (not shown). This proves that RuO_2 makes for a suitable Schottky contact to GaN which can be used to optically characterize semiconductor material without sacrificing its electrical properties.

6 References

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7 Appendix

7.1 Appendix A. Derivation of Current Transport Mechanism

If thermionic-emission is the limiting transport mechanism, only charged particles with energy greater than the barrier height can contribute to the current density [47]. Thus the carrier concentration in the bulk semiconductor is given by:

$$n = N_c \exp\left(\frac{-q(\phi_b - V_A)}{kT}\right) \quad (41)$$

Because the limiting cause is thermionic emission, one way of looking at the transmission of electrons is having a sharp step barrier much like that of what a metal electron see's at the boundary of the material. Instead of the vacuum level impeding electrons from leaving the substrate we can substitute the Schottky barrier (ϕ_b) and note that electrons will have a tunneling probability of p. Assuming that the semiconductor has a spherical constant-energy surface, the number a electrons per second that arrive at the boundary is $n\bar{v}/4$, where $\bar{v}$ is the mean Maxwellian distribution of velocity. The current density from electrons passing from the semiconductor to the metal then becomes:

$$J_{sm} = p\frac{qn\bar{v}}{4} = p\frac{qN_c\bar{v}}{4}\exp\left(\frac{-q(\phi_b - V_A)}{kT}\right) \quad (42)$$

Notice, that if at $V = 0$ the current density must go to zero, the current density from the metal to the semiconductor is:

$$J_{ms} = p\frac{qN_c\bar{v}}{4}\exp\left(\frac{-q\phi_b}{kT}\right) \quad (43)$$

So that

$$J(V_A) = J_{sm} - J_{ms} = p\frac{qN_c\bar{v}}{4}\exp\left(\frac{-q\phi_b}{kT}\right)\left\{\exp\left(\frac{qV_A}{kT}\right) - 1\right\} \quad (44)$$

Finally, if the scenario where the barrier becomes infinitely small is considered, then all of the electrons hitting the surface of what was the barrier will be transmitted through with a probability of $p = 1$. This scenario comes with the assumption that the value of $n\bar{v}/4$ will not change. Substituting $p = 1$ and $N_c = 2\left(\frac{2\pi m^* kT}{h^2}\right)^{\frac{3}{2}}$ into the above equation provides the IV characteristic of a thermionic-emission limited SB:

$$J(V_A) = A^* T^2 \exp\left(\frac{-q\phi_b}{kT}\right)\left\{\exp\left(\frac{qV_A}{kT}\right) - 1\right\} \quad (45)$$

Where

$$A^* = \frac{4\pi m^* q k^2}{h^3} \quad (46)$$

Table 7. Experimental Values of A* [65]

Semiconductor	A^* $(A\ cm^{-2}K^{-2})$
n-Si	$112(\pm 6)$
p-Si	$32(\pm 2)$
n-GaAs	$4-8, 0.41(\pm 0.15)$
p-GaAs	$7(\pm 1.5)$
n-GaN [91]	$29(\pm 6)$
Au/n-GaN	0.006[92], 14.68[93]
Pd/n-GaN	3.24d[93], 0.44[94]
Pt/n-GaN	6.61 [95], 64.7[94]

The previously derived function for current density is idealized and assumes that the barrier height has no dependence on the applied bias. In most fabricated Schottky barriers, this is not the case and the effective barrier height due to image barrier lowering can be written as $\phi_e = \phi_b - \Delta\phi_{bi}$, where $\Delta\phi_{bi}$ is the change of barrier height from image barrier lowering and can be seen in Figure 9.

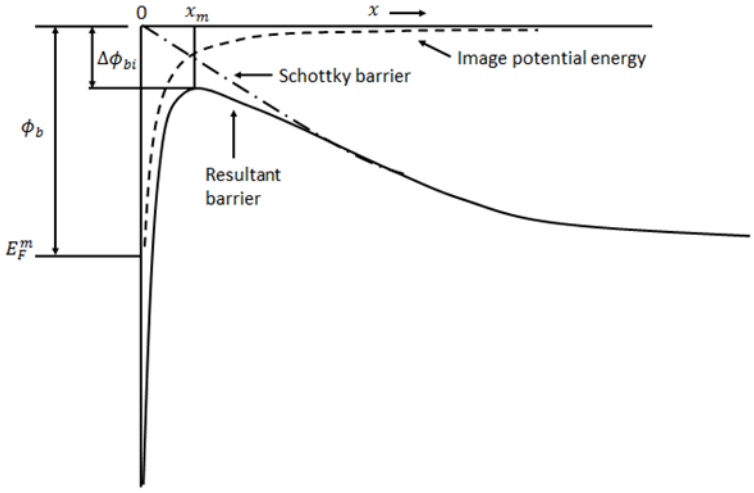

Figure 2. Image-force lowering of SB [52]

There also exists an interfactial layer whose dependance on the bias voltage changes the effective barrier height so that ϕ_e actually has two voltage dependent terms. The second one, if considered linear with voltage, can be expressed as βV where β is a constant. We can now write the effective barrier height as $\phi_e = \phi_{b0} - (\Delta\phi_{bi})_0 + \beta V$ where ϕ_{b0} and $(\Delta\phi_{bi})_0$ denote the respective barrier at zero bias and the voltage dependance is lumped into the βV term. Using the thermionic-emission current density derived above we can subsitute ϕ_e for ϕ_b which becomes:

$$J(V_A) = A^* T^2 \exp\left(\frac{-q(\phi_{b0} - (\Delta\phi_{bi})_0 + \beta V_A)}{kT}\right)\left\{\exp\left(\frac{qV_A}{kT}\right) - 1\right\} \qquad \textbf{7-1}$$

Which simplifies to,

$$J(V_A) = A^* T^2 \exp\left(\frac{-q(\phi_{b0} - (\Delta\phi_{bi})_0)}{kT}\right)\exp\left(\frac{-q\beta V_A}{kT}\right)\left\{\exp\left(\frac{qV_A}{kT}\right) - 1\right\} = J_0 \exp\left(\frac{-q\beta V_A}{kT}\right)\left\{\exp\left(\frac{qV_A}{kT}\right) - 1\right\}$$

Where

$$J_0 = A^* T^2 \exp\left(\frac{-q(\phi_{b0} - (\Delta\phi_{bi})_0)}{kT}\right) \qquad \textbf{7-2}$$

Note that if there is only ideal thermionic-emission across the barrier from the semiconductor to the metal and no effect from a voltage-dependent barrier height then $\beta \to 0$. If we want a measure of the deviation of β, we can define $\frac{1}{n} = 1 - \beta$ where n is the ideality factor and essentially corrects the current density equation for any deviations from the ideal equation. Thus after substituting $\beta = 1 - \frac{1}{n}$ the new form is:

$$J(V_A) = J_0 \exp\left(\frac{qV}{nkT}\right)\left\{1 - \exp\left(\frac{-qV_A}{kT}\right)\right\} \qquad \textbf{7-3}$$

7.2 Appendix B. Ni/GaAs Fabrication Process

7.2.1 GaAs Cleaning

A pre-fabrication cleaning is done to remove any organics or surface debris along with removing any surface oxide that may have formed after growth. Each sample was placed in a beaker of acetone for 10 minutes, then isopropyl alcohol (IPA) for 10 minutes, followed by a rinse in deionized water then blown dry in dry nitrogen. A dip in diluted hydrofluoric (10:1) acid for 1.5 minute and a deionized water rinse with nitrogen air dry was used to remove any thin film surface oxide. Finally, samples were dehydrated on a hot plate at 124˚C for 5 minutes.

Sample cleaning was also done before and after each electron beam metallization and dry etching step. To remove any residual photoresist, a plasma ashing step was executed under an oxygen ambient for 10 seconds. The samples were again dipped in HF for 1 minute, rinsed in DI water and blown dry with nitrogen. Following the drying step, samples were immediately mounted and taken to the next tool. The HF dip was not executed if any deposited metal was exposed on the sample surface.

7.2.2 GaAs Photoprocess

The AZ9260 i/h-line photoresist was used as both a metallization liftoff mask and an etching mask during sample fabrication. After dehydration, each sample was spun at 1000 RPM while the photoresist was dispensed and then immediately at 3000 RPM for 45 seconds. The softbake procedure was carried out at 115˚C for 3.5 minutes resulting in an average photoresist thickness of 8µm. A broadband UV exposure for 42 seconds was executed in a hard contact configuration for each field. Finally, samples were submerged in a 1:3 solution of AZ400K potassium-based developer and deionized water for 5 minutes.

7.2.3 GaAs Dry Etching

Although later GaN Schottky samples lacked the higher doped ohmic contact layer thus not requiring a dry etch step to access it, dry etching was carried out on the GaAs Schottky samples. The AZ9260 photoresist was used as an etch mask to create circular mesas. The mesa top is the unetched surface while the bottom is the exposed ohmic layer as seen in Figure 14 above. The etching recipe can be found in Appendix C.

7.2.4 GaAs Metal Deposition

All metal contacts were deposited by a Kurt Lesker PVD250 electron-beam evaporator under vacuum. Pattern formation was by photoresist lift-off. Based on work done by Matino et al. [96], a Sn(265nm)/Ag(10nm)/ Sn(265nm)/Ag(10nm)/Sn(265nm) stack was deposited and annealed to serve as an ohmic contact. The thickness of each layer was targeted to create a 96.5% Sn to 3.5% Ag by weight alloy which can be annealed at lower temperatures. Additionally, a stack of Ni(50nm)/Ag(500nm) was deposited on top of the ohmic contact to serve as a diffusion barrier and contact probe pad. The samples were anneal at 320˚C under He/Ar forming gas. Schottky contacts were formed by depositing 150nm of Ni and then 300nm of Ag. The sample was not annealed after Schottky contact deposition.

7.2.5 Step by Step Ni/GaAs Process

Step	Process Step	Description	Notes
1	Cleaning	Acetone Soak	10 min
		IPA Soak	10 min
		Di Rinse + N_2 Dry	-
		Oxide Removal	BOE (10:1) for 1 min
		Di Rinse + N_2 Dry	-
		Dehydrate	5 min at 124˚C
2	Photoprocess (Mesa Etch)	Photoresist Spin	1000 RPM Deposition 15 Sec 3000 RPM Spin 45 Sec
		PR Soft Bake	115˚C for 3.5 min
		PR Exposure	Broadband UV for 42 sec
		PR Develop	AZ400K:DiH_20 (1:3) for 5 min
		Ashing	Plasmatics 5 sccm O_2 for 10 sec
3	Cleaning	Acetone Soak	10 min
		IPA Soak	10 min
		Di Rinse + N_2 Dry	-
		Dehydrate	5 min at 124˚C
4	Photoprocess (Ohmic Contacts)	Photoresist Spin	1000 RPM Deposition 15 Sec 3000 RPM Spin 45 Sec
		PR Soft Bake	115˚C for 3.5 min
		PR Exposure	Broadband UV for 42 sec
		PR Develop	AZ400K:DiH_20 (1:3) for 5 min
		Ashing	Plasmatics 5 sccm O_2 for 10 sec
		Oxide Removal	BOE (10:1) for 1 min
5	Metallization	Ohmic Metal Deposition	Sn(265nm)/Ag(10nm)/ Sn(265nm)/Ag(10nm)/ Sn(265nm)/Ni(50nm)/Ag(500nm)
6	Lift-off	Acetone + Ultrasonic	~15 sec
7	Cleaning	Acetone Soak	10 min
		IPA Soak	10 min
		Di Rinse + N_2 Dry	-
		Dehydrate	5 min at 124˚C
8	Annealing	Annealing	320˚C for 5 min Under He/Ar
9	Cleaning	Acetone Soak	10 min
		IPA Soak	10 min
		Di Rinse + N_2 Dry	-
		Dehydrate	5 min at 124˚C
10	Photoprocess (Schottky Contacts)	Photoresist Spin	1000 RPM Deposition 15 Sec 3000 RPM Spin 45 Sec
		PR Soft Bake	115˚C for 3.5 min
		PR Exposure	Broadband UV for 42 sec
		PR Develop	AZ400K:DiH_20 (1:3) for 5 min
		Ashing	Plasmatics 5 sccm O_2 for 10 sec
		Oxide Removal	BOE (10:1) for 1 min
11	Metallization	Schottky Contact Dep.	Ni(150nm)/Ag(300nm)
12	Lift-off	Acetone + Ultrasonic	~15 sec
13	Cleaning	Acetone Soak	10 min
		IPA Soak	10 min
		Di Rinse + N_2 Dry	-
		Dehydrate	5 min at 124˚C

7.3 Appendix C. GaAs RIE Dry Etch Recipe

Trion RIE GaAs Dry Etch Recipe	
Pressure	10 mTorr
ICP Power	320 W
RIE Power	50 W
He Backflow Pressure	9 Torr
BCl_3 Flow Rate	20 sccm
Cl_2 Flow Rate	3 sccm
Chuck Temperature	20C
E-Static Voltage	600V
Etch Rate	1.58 µm/min

7.4 Appendix D. Metal/GaN Fabrication Process

7.4.1 GaN Cleaning

Similar to the GaAs process, a pre-fabrication cleaning is necessary to remove any surface contaminants present after MOCVD growth. Each sample was first soaked for 5 minutes in an aqua regia mixture made from a 3:1 solution of HCl to HNO_3 to remove any thin oxide films. Next the samples were ultrasonically cleaned in acetone for 5 minutes. A second aqua regia solution was made and the samples were soaked for 10 minutes. Samples were then moved a container of hydrofluoric acid (50%) for 10 minutes before being rinsed in deionized water and blown dry with nitrogen. Finally the samples were dehydrated at 124C for 5 minutes.

As with the GaAs process, a pre and post metal deposition cleaning was carried out. A 10 second oxygen plasma was used to remove any residual photoresist followed by a 1 minute BOE dip to remove any surface oxide. Once rinsed with deionized water and blown dry with nitrogen, the samples were immediately mounted into the e-beam vacuum chamber. If metal deposited during subsequent steps was exposed the pre-metallization clean consists of only a rinse in deionized water followed by being blown dry with nitrogen.

7.4.2 GaN Photoprocess

The photoprocess used for GaAs was used for GaN samples without change.

7.4.3 GaN Metal Deposition

All metal contacts were deposited by a Kurt Lesker PVD250 electron-beam evaporator under vacuum. Pattern formation was by photoresist lift-off. The ohmic contact stack consisting of Ti(30nm)/Al(400nm)/Ni(50nm)/Ag(300nm) was deposited without breaking vacuum. The Ti/Al layer is able to pin the Fermi level of the GaN to a point where tunneling occurs due to the nitrogen extracted from the surface [97]. The Ni/Ag layer acts as a metallic thermal diffusion barrier and a low resistance contact probe pad. The samples were annealed at 600C for 5 minutes after a lift-off and cleaning procedure.

The following Schottky metals were deposited on separate GaN samples: Pt(50nm), Ru(50nm), Au(50nm), Ni(50nm), RuO_2(10nm), Ni(5nm)/Au(5nm), Ru(5nm)/Ni(5nm), and Annealed Ni(10nm). The Ni/Au and Annealed Ni samples were annealed at 500C for 3 minutes in open air while the Ru/Ni and RuO_2 samples were annealed at 600C for 3 minutes in open air. No other samples were annealed after Schottky metal deposition. An ohmic contact pad of Ni(50nm)/Ag(300nm) was deposited on top of the Schottky metal.

7.4.4 Step by Step Metal/GaN Process

Step	Process Step	Description	Notes
1	Cleaning	Aqua Regia Soak	5 min
		Acetone + Ultrasonic	10 min
		Aqua Regia Soak	10 min
		HF (50%) Soak	10 min
		Di Rinse + N_2 Dry	-
		Dehydrate	5 min at 124˚C
2	Photoprocess (Ohmic Contacts)	Photoresist Spin	1000 RPM Deposition 15 Sec 3000 RPM Spin 45 Sec
		PR Soft Bake	115˚C for 3.5 min
		PR Exposure	Broadband UV for 42 sec
		PR Develop	AZ400K:Di$H_2$0 (1:3) for 5 min
		Ashing	Plasmatics 5 sccm O_2 for 10 sec
		Oxide Removal	BOE (10:1) for 1 min
3	Metallization	Ohmic Metal Deposition	Ti(30nm)/Al(400nm)/ Ni(50nm)/Ag(300nm)
4	Lift-off	Acetone + Ultrasonic	~15 sec
5	Cleaning	Acetone Soak	10 min
		IPA Soak	10 min
		Di Rinse + N_2 Dry	-
		Dehydrate	5 min at 124˚C
6	Annealing	Annealing	600˚C for 5 min Under He/Ar
7	Cleaning	Acetone Soak	10 min
		IPA Soak	10 min
		Di Rinse + N_2 Dry	-
		Dehydrate	5 min at 124˚C
8	Photoprocess (Schottky Contacts)	Photoresist Spin	1000 RPM Deposition 15 Sec 3000 RPM Spin 45 Sec
		PR Soft Bake	115˚C for 3.5 min
		PR Exposure	Broadband UV for 42 sec
		PR Develop	AZ400K:Di$H_2$0 (1:3) for 5 min
		Ashing	Plasmatics 5 sccm O_2 for 10 sec
		Oxide Removal	BOE (10:1) for 1 min
9	Metallization	Schottky Contact Dep.	-
6	Annealing	Annealing	RuO_2 and Ru/Ni Schottky: 600˚C for 5 min in open Air Annealed Ni and Ni/Au Schottky: 500˚C for 5 min in open Air
10	Lift-off	Acetone + Ultrasonic	~15 sec
11	Cleaning	Acetone Soak	10 min
		IPA Soak	10 min
		Di Rinse + N_2 Dry	-
		Dehydrate	5 min at 124˚C
12	Photoprocess (Contact Pads)	Photoresist Spin	1000 RPM Deposition 15 Sec 3000 RPM Spin 45 Sec
		PR Soft Bake	115˚C for 3.5 min
		PR Exposure	Broadband UV for 42 sec
		PR Develop	AZ400K:Di$H_2$0 (1:3) for 5 min
13	Metallization	Ohmic Metal Deposition	Ni(50nm)/Ag(300nm)
14	Lift-off	Acetone + Ultrasonic	~15 sec
15	Cleaning	Acetone Soak	10 min
		IPA Soak	10 min
		Di Rinse + N_2 Dry	-
		Dehydrate	5 min at 124˚C