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The performance of thin-film GaN Schottky diodes fabricated using a large-area epitaxial lift-off (ELO) process is reported in this work. Comparison of the device characteristics before and after lift-off processing reveals that the Schottky barrier height remains unchanged by the liftoff processing and is consistent with expectations based on metal-semiconductor work function differences, with a barrier height of approximately 1 eV obtained for Ni/Au contacts on n^- GaN. However, the leakage current in both reverse and low-forward-bias regimes is found to improve significantly after ELO processing. Likewise, the ideality factor of the Schottky diodes also improves after ELO processing, decreasing from $n = 1.12–1.18$ before ELO to $n = 1.04–1.10$ after ELO. A possible explanation for the performance improvement obtained for Schottky diodes after substrate removal by ELO processing is the elimination of leakage paths consisting of vertical leakage along threading dislocations coupled with lateral conduction through the underlying n^+ buffer layer that is removed in the ELO process. Epitaxial liftoff with GaN may enable significant improvement in device performance and economics for GaN-based electronics and optoelectronics. *Published by AIP Publishing.*
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The unique material properties of GaN and related III-N semiconductors, such as a high critical electrical field, large band gap, high saturation electron velocity, good electron mobility, and high thermal conductivity,[1,2] have made GaN and related materials one of the most promising material systems for high-performance optoelectronics as well as next-generation power electronics. Despite the inherent material advantages of GaN and numerous device demonstrations, the actual performance of many lateral GaN devices has fallen short of the ultimate performance expected from the consideration of fundamental material parameters. These performance discrepancies, which include effects such as large ideality factors, higher-than-expected reverse saturation currents, inability to support avalanche currents in diodes,[3,4] and the presence of surface- and/or buffer-related effects such as dynamic on-state resistance, current-collapse, and hysteresis in FETs,[5,6] have thus far limited the applications that can be addressed using GaN electronics. The use of lattice-mismatched non-native GaN substrates (driven by the high cost and limited availability of native GaN substrates) also results not only in large dislocation densities but also in limited thermal conductance for through-substrate heat removal.[7,8] As is well known, power devices are typically thermally limited[9,10] so that the die size is set by power dissipation and thermal resistance considerations, rather than by current density limitations.

Epitaxial lift-off (ELO) processing offers an alternative approach to address these issues. By reducing the effective substrate thickness to near zero (by removing the substrate and mounting the resulting thin-film device directly on a heat sink), the use of ELO processing provides a path to smaller die sizes and lower cost and (as will be discussed) can also result in improved device performance. As an exploration of the potential of ELO processing, we present a comparative study of lateral Schottky diodes on n^- GaN, fabricated with and without ELO processing. It is observed that ELO processing improves the device characteristics relative to the as-fabricated devices (prior to ELO processing) for materials grown on a sapphire substrate. A reduction in leakage current and improved device characteristics are observed after lift-off and transfer to an insulating host substrate.

Lift-off processing of GaN films has been demonstrated by several techniques, including laser lift-off,[11] selective etching of release layers,[12–14] substrate removal,[15] and band gap selective photoelectrochemical (PEC) etching techniques.[16,17] In this work, a band gap selective PEC technique is used.

The devices reported here are illustrated schematically in Fig. 1. The device structure includes a 2 μm thick n^+ GaN buffer layer (Si, 3×10^{18} cm^{-3}), an undoped pseudomorphic InGaN release layer (<0.1 μm thick to retain crystal quality), and a 5 μm n^- GaN device layer (Si, nominally 2×10^{17} cm^{-3}). Diodes were fabricated on the as-grown epitaxial wafer structures, followed by PEC wet-processing-based lift-off. Processing was performed on quarters of 100 mm diameter wafers to illustrate the scalability of the processing. The fabrication of the planar Schottky diodes included n-type ohmic metallization (30/100/50/50 nm Ti/Al/Ni/Au deposited by electron-beam evaporation and lift-off, followed by rapid thermal annealing at 750 °C for 3 min in N_2), and Schottky contacts formed by evaporation and lift-off of 40/100 nm Ni/Au. Prior to epitaxial lift-off, the devices were encapsulated in a 25 μm thick metal support layer to provide protection as well as mechanical support during handling.

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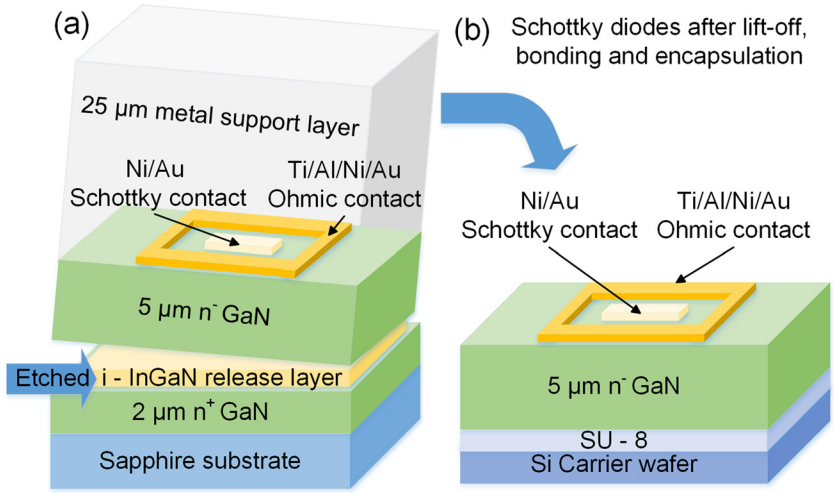

FIG. 1. Schematic structure of the Schottky diode (a) before and (b) after ELO processing.

The epitaxial lift-off process used is a wavelength-selective wet-chemical photoelectrochemical (PEC) etch based on the use of a high-power light-emitting diode (LED)-based UV light source with peak irradiance at a photon energy below the band gap of GaN to ensure that optical absorption occurred primarily in the InGaN release layer. The PEC lift-off process is performed in a KOH solution, with the sample acting as the anode, and a Pt wire as the cathode of the resulting electrochemical cell. The UV illumination acts to drive the electrochemical dissolution reaction. The sample is illuminated through the substrate (i.e., from the back) to facilitate undercut etching of the InGaN release layer. After epitaxial lift-off, the thin-film device layers were bonded to a Si carrier wafer using SU-8, and the metal support layer and associated seed were removed by selective wet-chemical etching. The details of this PEC release process have been previously reported.[18–20]

Diodes were tested directly after fabrication (prior to ELO processing) as well as after the ELO substrate removal and carrier wafer bonding process. Fig. 2 shows a typical set of room-temperature current-voltage (I-V) characteristics for the same device with a 40×40 μm^2 active area before and after epitaxial lift-off. The spacing between anode and cathode contacts is 10 μm. The turn-on voltage is consistent with the theoretical expectation of 1.0 eV from the Ni/Au Schottky contact on GaN if the work function of Ni and the electron affinity of n-type GaN are 5.1 and 4.1 eV, respectively.[21,22] For a reverse bias voltage of −15 V (corresponding to an average depletion-region electric field of 545 kV/cm as estimated from the numerical simulation of Poisson's equation for the device structure in Fig. 1), the measured reverse current density is 7.2×10^{-2} and 4.0×10^{-3} A/cm^2 for devices before and after ELO processing, respectively. Under forward bias, the as-fabricated devices exhibit two distinct regions: a leaky low-bias region for biases below 0.4 V and a more ideal diode region at higher biases. In contrast, the leaky low-bias region is eliminated in the characteristics measured after lift-off, as shown in the upper-right inset of Fig. 2.

To obtain additional insight into the physics underpinning these results, variable temperature characterization and modeling of these GaN Schottky diodes have been performed. For the measurements reported here, the temperature was set using the chuck of a variable-temperature wafer probe station. The measured reverse-bias *I-V* characteristics over temperature of as-fabricated and ELO-processed GaN Schottky diodes are shown in Fig. 3. For the full range

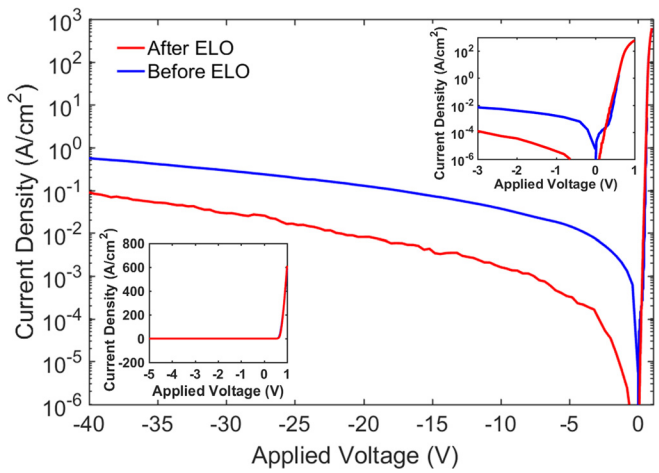

FIG. 2. Semi-log plot of typical room-temperature I-V characteristics of the GaN Schottky diode before and after lift-off processing. The insets show the details near the origin on a semi-log scale, as well as the I-V characteristics on a linear scale.

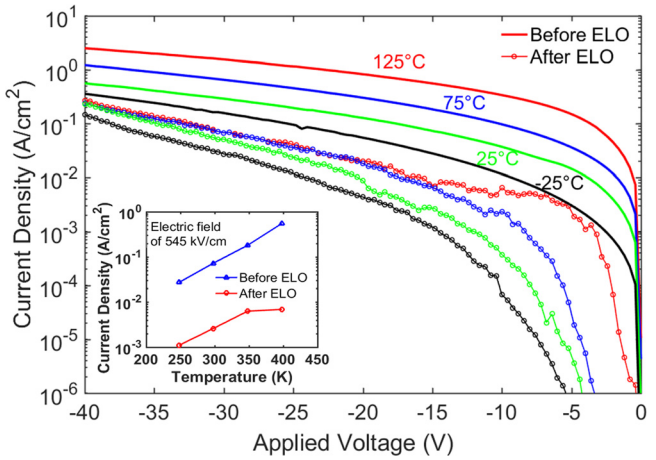

FIG. 3. Semi-log plot of the reverse-bias I-V characteristics as a function of temperature for GaN Schottky diodes before and after epitaxial lift-off processing.

of temperatures evaluated (−25 C to +125 C), the reverse current is lower for devices after ELO processing. For ideal Schottky diodes, the characteristics are expected to be dominated by thermionic emission, although other phenomena such as field-assisted tunneling through the barrier and trap-assisted and thermionic generation in the depletion region may contribute to the deviation from these expectations.[23,24] For ideal devices dominated by thermionic emission,

$$I = I_O\left[\exp\left(\frac{qV}{nkT}\right) - 1\right], \tag{1}$$

$$I_O = AA^{**}T^2\exp\left(\frac{-q\phi_B}{kT}\right), \tag{2}$$

where ϕ_B is the Schottky barrier height, k is the Boltzmann constant, n is the ideality factor, I_O is the reverse saturation current, A is the contact area, and A^{**} is the effective Richardson constant. As shown in the inset of Fig. 3, the reverse current density at 545 kV/cm is much lower after ELO and exhibits a significantly reduced temperature dependence.

The measured I-V vs. temperature characteristics under forward bias are shown in Fig. 4. As can be seen, the turn-on voltage increases as the temperature is reduced, as expected for thermionic emission. In addition, the ELO-processed devices have a modestly higher turn-on voltage than the as-fabricated devices and also exhibit a much lower leakage current density, reaching the measurement noise floor ($\sim 3\times10^{-9}$ A/cm^2) for the −25 °C case at voltages below 0.25 V. Fig. 4 shows that the ELO process effectively removed the excess forward bias leakage current that is evident in the as-fabricated device measurement results. The ideality factor and ϕ_B can be extracted from the intercepts and slopes of the linear part of the characteristics shown in Fig. 4. The ideality factor improved from 1.12 to 1.18 before ELO processing to from 1.04 to 1.10 after ELO processing, and the ϕ_B value for both pre- and post-ELO devices is close to the theoretical value obtained from the difference between the Ni work function and GaN electron affinity[25,26] as shown in Table I. As an additional check, the modified Norde method was applied to extract ϕ_B since the extrapolated I_O from the I-V vs. temperature plot can be unreliable for small

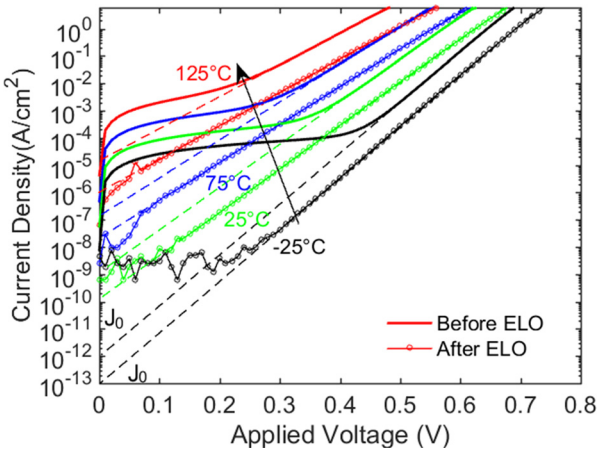

FIG. 4. Semi-log plot of the forward-bias I-V characteristics as a function of temperature for GaN Schottky diodes before and after epitaxial lift-off processing.

TABLE I. Comparison of barrier heights and ideality factors over temperature for Schottky diodes before and after ELO processing.

	T (°C)	n	ϕ_B I-V (eV)	ϕ_B *Norde* (eV)
Before ELO	125	1.18	0.99	0.99
	75	1.16	0.89	0.90
	25	1.13	0.91	0.95
	−25	1.12	0.87	0.96
After ELO	125	1.10	0.99	0.99
	75	1.08	0.99	1.00
	25	1.05	0.91	0.95
	−25	1.04	0.94	1.00

applied voltages or if there is appreciable recombination current or series resistance.[27] The Norde function $F(V)$, defined by[28]

$$F(V) = \frac{V}{2} - \frac{kT}{q}\ln\left(\frac{I}{AA^{**}T^2}\right), \tag{3}$$

is plotted in Fig. 5. The applied voltage V_O corresponding to the minimum of the Norde function can be used to extract ϕ_B using[21]

$$\phi_B = F(V_O) + \frac{V_O}{2} - \frac{kT}{q}. \tag{4}$$

For ELO-processed diodes, as shown in Fig. 5, $F(V)$ depends linearly on V for low voltage except for the $V < 0.25$ V region at −25 °C where the true device current is obscured by the measurement noise floor. However, the as-fabricated diodes exhibit leaky low-bias regions. This contributes to the additional minima in F(V) observed for V ≤ 0.1 V in Fig. 5, which thus should not be considered when extracting V_0. For large V, $F(V)$ approaches a straight line with a slope of 1/2 as expected in Eq. (3) for all the devices evaluated. Table I compares the ideality factors and extracted barrier heights for diodes before and after lift-off over temperature. As shown in Table I, the barrier height values agree well with the theoretical expectations for Ni/GaN contacts across both the methods used and the full temperature range evaluated, and the ideality factors are well behaved, suggesting that the diode behavior is nearly ideal. It should be noted that for the data in Figs. 3–5, the self-heating of the device is estimated to be below 0.5 K from the estimates of the thermal conductivity of the substrates and the low power dissipation in the devices.

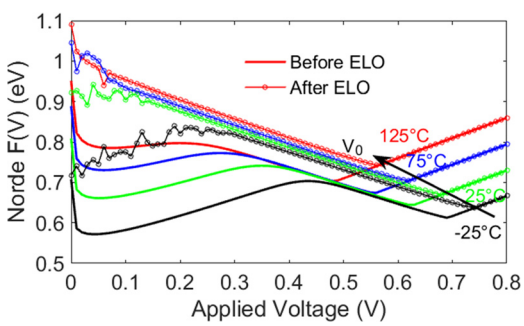

FIG. 5. Plot of the Norde function over bias and temperature, to facilitate barrier height extraction.

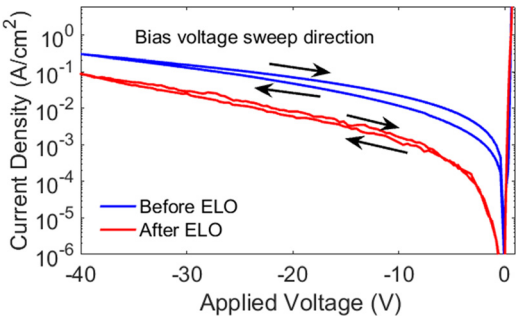

FIG. 6. Cyclic I-V measurement at a scan rate of 1 V/s.

The cyclic I-V measurement with a voltage sweep rate of 1 V/s and the cyclic C-V measurement with a voltage sweep rate of 0.2 V/s were performed to look for hysteresis as a signature of trapping in the devices. As shown in Fig. 6, a small amount of I-V hysteresis was apparent in the as-fabricated devices; this disappeared after ELO processing. For the C-V measurements (not shown), no hysteresis was found in either case. The C-V characteristics were also used to validate the doping concentration in the epitaxial layers,[29,30] with geometric edge corrections applied due to the small device area.[31,32] The obtained doping concentration was found to be uniform through the depletion layer thickness and unchanged before and after ELO processing, with a value of approximately 2.5×10^{17} cm^3. In addition, variable-frequency C-V measurements from 2 kHz through 1 MHz were performed before and after ELO processing, as shown in Fig. 7. As expected for Schottky diodes, no frequency dispersion was observed, and no significant differences between the C-V characteristics before and after ELO processing could be discerned. These observations suggest that ELO processing does not have a discernible impact on bulk material properties or trap generation but does reduce the leakage current. Further details on material-level characterization can be found in Ref. 20; no clear differences in material quality before and after lift-off processing could be detected.

As noted above, devices exhibit substantially reduced leakage after lift-off processing in both the reverse and low forward bias conditions. On the other hand, the Schottky barrier height is found to be constant, while the ideality factor improves after liftoff. Fig. 8 illustrates schematically a proposed mechanism to explain these observations. These GaN

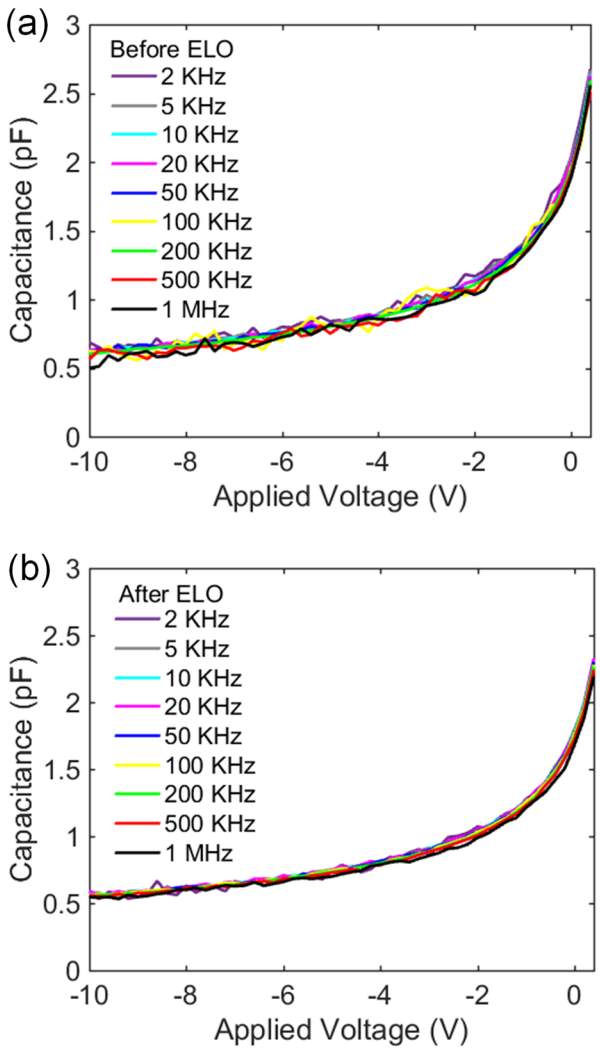

FIG. 7. Measured C-V characteristics (a) before ELO and (b) after ELO processing. In both the cases, no frequency dispersion is observed, and no significant differences are seen before or after ELO.

based epitaxial films, grown on sapphire, contain a high density of dislocations. Leakage current paths associated with dislocations having screw character[33,34] have been observed previously. In the case of the Schottky diodes fabricated here, these conductive dislocations form shunt paths through the devices. These are shown, for illustration purposes, as the dashed gray vertical lines in Fig. 8. For the devices before

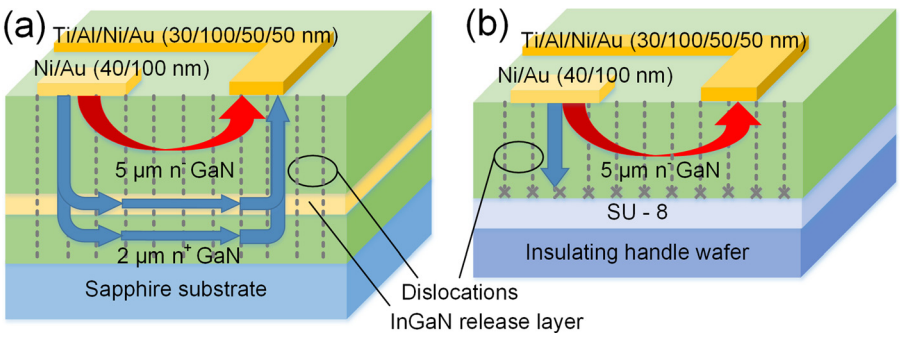

FIG. 8. Schematic illustration of the possible mechanism for the performance improvement in ELO-processed GaN Schottky diodes. The red arrow denotes the ideal thermionic Schottky current contribution, while the blue arrows illustrate the leakage paths. The leakage paths include a vertical component along dislocations, and a lateral component in the InGaN release layer quantum well and the n^+ GaN buffer. Elimination of these two layers, and replacement of them with an insulating bond and carrier wafer, eliminates this leakage mechanism.

ELO processing, these dislocations pass through the n^- GaN Schottky layer, through the InGaN release layer, and into the n^+ GaN buffer. This heavily doped buffer and the quantum well associated with the InGaN release layer can provide a low-resistance lateral current path between the vertical dislocations, as illustrated with the blue arrows in Fig. 8(a). In contrast, for the ELO-processed devices, the release layer and n^+ buffer are removed, eliminating this lateral path connecting the dislocation shunt paths. These leakage paths are thus "disconnected" by the insulating carrier wafer bond, eliminating the leakage path. As a consequence, the devices after epitaxial lift-off show more nearly ideal characteristics, as illustrated by the curved red arrows in Fig. 7.

In summary, we have investigated single-crystal thin-film GaN Schottky diodes fabricated using a photoelectrochemical wet-etch-based epitaxial lift-off process. Comparing the devices with and without ELO processing, we find that the ELO processing does not result in any detectable degradation of the GaN based material quality. Perhaps counter-intuitively, the leakage current and device electrical characteristics are improved after ELO processing, with improved ideality factor and greatly reduced reverse leakage currents; no significant change in the Schottky barrier height is observed. A physical mechanism that is consistent with the experimental observations is the elimination of dislocation-related leakage paths in the devices processed by ELO. The approach described here may be beneficial for GaN-based electronic and optoelectronic devices over a wide range of applications, while also providing a potential route to reuse of low-dislocation native GaN substrates. While the results reported here were obtained for GaN films on non-native substrates (i.e., sapphire), this approach could also be applied to devices grown on native GaN substrates, potentially enabling substrate reclaim and reuse.

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